FAIRLIGHT INSTRUMENTS

CMI DIAGNOSTIC SOFTWARE DESCRIPTION

Covering software for:-
Channel Card Tests
Master Card Tests
64K RAM Card Tests
Central Processor Control Module
Light Pen Interface
Graphics System
Floppy Disc Controller
Interrupt Tests - CMIINT
Testing a Complete CMI - Chain Tests

CAUTION: WHENEVER CHANGING OR REMOVING THE CMI MASTER CARD OR CHANNEL CARDS, OR PLUGGING RIBBON CABLE CONNECTORS ONTO THESE CARDS, ALWAYS SWITCH OFF POWER FIRST. FAILURE TO DO SO WILL ALMOST CERTAINLY CAUSE HARDWARE DAMAGE!

REVISION: 1.0

FEBRUARY, 1982

Table of Contents
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1.Ø General Introduction

This document describes the set of diagnostic test programs available on disc for testing and debugging all the plug-in circuit modules of the Fairlight Computer Musical Instrument.

1.1 Running the Diagnostic Disc

The diagnostics run under the QDOS operating system. They are therefore supplied on a QDOS system disc which should be loaded into the CMI instead of the usual CMI system disc immediately after power-up or RESTART.

As soon as the disc drive door is closed, the CMI will load QDOS automatically and display a sign-on message giving version and revision numbers.

The QDOS prompt will then be displayed. This is just an equals sign "=" on a line of its own. This indicates that the computer is ready to accept a command.

For further details of the QDOS operating system features, refer to the QDOS User's Guide.

1.2 Running the Test Programs

Most of the diagnostic programs make use of a common command interpreter for operator control, so there is a uniform command syntax employed throughout, and several test options available as standard. Tests may be run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

where the <test name> is as described in each section. Options are of the form

<O>=n where <O> is a single character and n is an integer.

Standard options are

P=n Repeat test command n times. Using "C" instead of an integer initiates continuous testing.

N=n Select test number n. There are usually several test commands with the same name. By default, all tests are executed sequentially but single tests or subsets of the available tests can be specified.

e.g. N=1 Test no. 1 only
N=1,3,5 Tests 1, 3 and 5
N=4-7 Tests 4 to 7 inclusive

Some tests, which require a waveform to be observed, wait for the spacebar to be pressed

before terminating or proceeding to the next test.

To obtain a reminder of what tests are available from the current test program being run, type

LIST<CR>

To repeat the last test, just type

R<CR>

If an error condition occurs, a moderately helpful message is printed on the console and the program returns to the command interpreter. Successful tests terminate without comment and return to the interpreter or proceed to the next test as soon as completed. Certain tests require the user to check waveforms with an oscilloscope and will not terminate or proceed to the next test until the spacebar is pressed.

Measurement Tolerances

A tolerance of +/- 15% is acceptable for most voltage or frequency measurements. Filter attenuation levels are harder to control and may be subject to +/- 20% variation.

Changes to analog circuitry in design revisions may also effect level measurements. Values quoted here are valid for the revisions referred to in the text.

2.Ø Channel Card Tests

A program for testing CMI channel cards is CMITST.CM which can be run by typing

CMITST

with the CMI diagnostics disc in drive Ø.

It can test channel cards individually or up to eight at a time. There are eight different tests within CMITST, which each exercise a different part of the channel card.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

A "C=n" option is avilable for all tests, which specifies the channel number(s)to be tested, in the range 1 to 8. Default is 1. Multiple channel numbers can be specified separated by commas or a hyphen.

e.g. FILT;C=3
FILT;C=1-4
FILT;C=3,5

One side of the balanced analog output of the channel card is available at test point 6 (TP6) at the front of the card. The row of test pins is numbered from 1 at the bottom. Pins 1 and 2 are connected to digital ground, 3 and 4 to analog ground.The other side is available at test point 5. Measurements quoted in this text refer to TP6. However if a complete CMI is being tested, it may be more convenient to use the Fairlight Analog Tester box (see section 1Ø.3 for how to connect it to the CMI and an oscilloscope). Waveforms observed from the tester will be of the same form as TP6 but different levels. Refer to the Waveform Summary (section 11) for Analog Tester levels.

Note that Fairlight DO NOT release schematics of the Channel Card as all repairs are done on a return-to-factory basis.
For in-house use by Fairlight, refer to:
"Channel Card Description"
Channel card schematics CMI-Ø1-Ø1 to CMI-Ø1-Ø4
Channel card component location diagram

Board component references are for the Revision 7 channel

card and this section describes CMITST Revision 1.3

2.1 Filter Tests

Test name: FILT
No. tests: 15
Purpose: Tests the basic playback facility of the channel card and the software-controlled tracking filter.

For each test a fundamental sine wave is loaded into two segments of waveform memory, and a program-specified harmonic is loaded into the following two segments. Timers 1 and 2 are disabled (for no envelope modulation) and timer 3 is initialised to count 4 segments. The segments are then replayed continuously (by segment looping) with the tracking filter cutoff set to achieve approximately a 2:1 attenuation between the fundamental and harmonic. The output level of the fundamental at TP6 should be 3.4V p-p. The digital control to the filter is latched by IC C9 when the LAT2 address is decoded.

After each of the 15 tests the program will halt until the space bar is hit so that the channel card output can be observed.

Test name: FILTD
No. tests: 3
Purpose: Tracking filter test with operator settable parameters.
Options: F=n Filter setting. Range 1-15, default 8
H=n Harmonic number. Range 1-32, default 16

This is basically the same as FILT, but with additional operator control. The fundamental used for tests 1-3 are 200Hz, 1000Hz, and 5000Hz respectively. The same frequncy shifting is used as in the FILT test, but the harmonic may be specified by the user as a multiple of the fundamental, as can the filter setting.

2.2 Waveform Memory Tests

Test Name: MEM
No. tests: 8

Test No.1 - "Read-write Ø"
Purpose: Tests memory read-write ability.
First the waveform address counters are reset (G1-G3) then the entire memory is written with zeros. The address count is automatically incremented after each write by having LOAD asserted and RUN not asserted. Memory is read back in the same way to verify data.

Test No.2 - "Read-write FF"
Purpose: Tests memory read-write ability.
Writes $FF sequentially to entire memory and reads back to verify as in test 1.

Test No.3 - "Read-write and Refresh AA"
Purpose: Tests memory read-write ability.
Writes $AA to the entire memory, executes a delay loop for 5 seconds then verifies the contents of memory as in test 1.

Test No.4 - "Channel-Segment-Byte Uniqueness Forward"
Purpose: Checks that each byte in 16K memory of each channel card being tested can be addressed uniquely.
Memory is filled with 4-byte uniqueness patterns. Each pattern consists of the channel mask selecting that channel, the segment number being written to, and the double-byte offset of the first byte in the pattern.
Each channel memory is then read back in the same order to verify the patterns.

Test No.5 - "Channel-Segment-Byte Uniqueness Reverse"
Purpose: Addressing uniqueness.
This test is identical to No. 4 except that channel memories are filled beginning with channel 8 instead of channel 1. This in case a fault on channel 1 is causing a fault to appear on another channel.

Test No.6 - "Segment Random Access using Load"
Purpose: Tests ability to preset waveform segment counters.
Waveform segment counters (ICs G1,G3) are preset from the WS outputs of PIA FG5. This test can only be performed after test No.5 since it reads the uniqueness patterns to check that the correct segment has been selected.
A bit-swapping routine is used to generate a set of 127 non-sequential segment numbers. Each segment preset is loaded when the LOAD signal (also from PIA) is toggled, and the second byte of the uniqueness pattern at that preset is read to check the segment number.

Test No.7 - "Segment Random Access using Run"
Purpose: Waveform segment presettability.
Tests waveform segment preset as in test 6 but preset is loaded when RUN signal toggles.

Test No.8 - "Sequential Access"
Purpose: Checks that segment 1 of each channel can be written with an incrementing pattern.
Writes to all channels simultaneosly from zero address through to the end of memory then reads back, starting with channel 1.

2.3 Envelope Control Tests

Test name: RAMP
No. tests: 4
Options: F=n Filter cutcff frequncy.
Range 1-15, default=15

Test No.1 - "Ramp Preset"
Purpose: Tests ability to preset the envelope-shaping DAC

The envelope DAC (IC G8) is preset from the RP outputs of PIA FG5. The waveform DAC is provided with a steady data input of $FF while its reference voltage (the envelope) is cycled linearly between Ø and $FF. The ramp up/down counters are preset on every segment from the PIA to drive G8 up and down. A low frequncy triangle waveform should result at TP6 with 1.75V p-p amplitude. Terminate test and advance to the next by hitting the space bar.

Test No.2 - "Ramp Auto Run"
Purpose: The envelope of each segment may be ramped individually by the up/down counters (G6, G7).

The ramping rate is controlled by timers 2 and 3 for even and odd segments respectively. In auto-run the counters are clocked as each timer times out and increment or decrement according to the DIR output from the PIA (FG5). The Terminal Ramp Interrupt (TRI) is generated whenever the counters reach Ø or $FF, whereupon the DIR bit is changed to ramp in the opposite direction. The result is a clipped triangle waveform, 1.75V p-p at TP6. Terminate test by hitting the space bar.

Test No.3 - "Force Ramp Up and Down"
Purpose: Checks ramp up/down override.

Ramp counters are allowed to ramp up and down as in test 2 but the DIR control is overridden by the Force Ramp Up (FRU) and Force Ramp Down (FRD) controls, which are asserted by accessing addresses $EØØ3 and $EØØ4 respectively.

The same clipped triangle waveform should appear at TP6. Terminate test by hitting the space bar.

Test No.4 - "Ramp Zero Offset"
Purpose: Checks for noise or a DC offset from envelope DAC at zero output.

The ramp level is preset to zero. There should be negligible cutput (less than 3ØØmV p-p) from the channel card at TP6.

2.4 Volume Control

Test name: VOL
No. tests: 2
Purpose: Checks volume control DAC.
Options: F=n Filter cutoff harmonic
Range 1-15, default 8
S=n Volume change speed
Range 1-127, default 1

The volume control DAC (F7) is the last stage in the audio processing system. With a DC reference (normally the envelope shaped and filtered waveform) volume data is cycled repetitively between zero and $FF. This data is latched directly from the buss through latch F6, addressed at $E001. The cycle speed is controlled by the S option: 1 corresponds to maximum speed.

A triangle waveform of 2V p-p should be observed at TP6. Terminate the test by hitting the space bar.

Test No.2 - "Zero Offset Test"
Purpose: This test checks the zero offset of the fixed low-pass filter which precedes the volume DAC.

The latched VOL level is set to zero. A trimpot should be available at the front of the channel card. If a buzzing sound occurs, accompanied by a small sawtooth waveform at TP6, adjust the trimpot until no buzzing is heard at max monitor volume. There should be no more than 300mV p-p of noise when the trimpot is set correctly. Terminate the test by pressing the space bar.

If no trimpot is on the board, refer to Field Change Notice 32.

2.5 Timer Tests

Test name: TIM
No. tests: 3

Test No.1 - "Timer Read/Write Latches"
Purpose: Checks ability to communicate with timer.
The 6840 timer (BC8) contains 3 16-bit timer counters and 3 associated preset latches. First all timers are held in preset state and outputs enabled by writing $81 to the internal control registers. Then timer 1 preset latch is written with all numbers from Ø to $FFFF and its associated timer read back for verification after each write. (In the preset state each counter reflects the contents of its preset latch). The other two timers are then tested in the same way.
Each write/read is a double-byte transfer through the 8-bit buss.

Test No.2 - "Timer Internal Clock Timeout"
Purpose: Checks timeout action using internal clock.
Timers are programmed to be decremented from the internal clock (provided by the E input, BCAS) and are all initialised to $FFFF. Timeout occurs when a timer decrements to zero. All three timers should timeout together. A software timer is used as a reference to detect early or missed timeouts. The 6840 status register is repetitively polled to check when timeout occurs.

Test No.3 - "Timer External Clock Timeout"
Purpose: Checks timeout action using external clock.
Clock timeout is verified using the external clock inputs. Timer 1 is clocked by BCAS divided by 8 (4uS intervals from E11), enabled by the non-assertion (high level) of LOAD, and is initialised to $FFFF/8. Timers 2 and 3 are clocked by BCAS/ and initialised to $FFFF/4 so using the same reference as test No.2, all three should timeout simultaneously.

2.6 Pitch and Octave Control

Test name: PIT
No. tests: 2

Test No.1 - "Octave Register"
Purpose: Checks accuracy of the octave control PIA.
With the pitch register (B4, C4 from PIA BC5) held at max, octave register (D7, also from BC5) is cycled from Ø to 8. At each setting, timer 3 is used to time a waveform by presetting a segment count appropriate to that octave and selecting the RUN mode. If timeout occurs before the End of Sound flag (EOSI) or if the timer value is greater than a certain tolerance when EOSI does occur, an error is generated. Timer is clocked by the internal clock (PCAS).

Test No.2 - "Pitch Register Test"
Purpose: Checks accuracy of pitch control from PIA.
With the octave register held constant, the 10-bit pitch register is cycled from zero to maximum and and the same method is used to verify the waveform accessing frequency as in test No.1.

2.7 Interrupt Flags

Test name: FLG
No. tests: 4

Test No.1 "End of Sound Flag"
Purpose: Test the "last segment" flag.
EOSI is generated when the waveform address counters (G1-G3) reach maximum. To test it, the segment count is preset to the last segment ($7F), and 127 writes to waveform memory are executed. On each write, premature EOSI is checked for. One more write should then produce EOSI.

Test No.2 "Terminal Ramp Flag"
Purpose: Test "clipping" flag.
Generated by zero or max count being reached by ramp counters (G7,G6). With DIR bit from PIA FG5 set to 1 (down), $80 is written to the ramp preset (RP) outputs of PIA FG5 and the status of PIA BC5 read to check for no TRI flag. Then zero is written to RP and BC5 read again to check that TRI is present. Each preset write is followed by a toggle of LCAD to latch the preset data on G6, G7.
The DIR bit is then cleared (ramp up) and $7F and $FF written to the ramp preset to clear and set the TRI flag respectively.

Test No.3 - "Zero Crossing Flag"
Purpose: Test "middle of segment" flag.
Generated at the middle of every segment by waveform address counter G2. ZX goes high when the within-segment byte count reaches 64 (so ZX bar generates a +ve edge at end of each segment). The test asserts LOAD to clear the counter then does 63 writes to waveform memory, checking each time that the flag is clear. One more write should then set ZX.

Test No.4 - "Zero Cross Interrupt Flag"
Purpose: Test "middle of last segment" flag.
Zero crossing interrupt (ZCINT) occurs on first zero crossing (ZX) after the timer 1 (segment counter/timer) timeout. Timer 1 is programmed to be clocked by the internal clock (RCAS). Until it times out, ZCINT is checked from PIA status to check there is no premature flag. After timeout plus a delay to allow for 120uS uncertainty in the arrival of ZX, the PIA is read again to check that ZCINT has occurred. The address counters are clocked at maximum pitch during the test.

3.0 Master Card Tests

The master card can be diagnosed using the program MAST.CM, run by typing

MAST<CR>

with the CMI diagnostics disc in drive 0.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

Some MAST tests require at least one channel card to be installed in the CMI. These are indicated by the presence of a C option in the descriptions below.

References:-

"CMI-02 Master Card Functional Description"
Drawings CMI-02-01 to CMI-02-04

Board component references apply to the Revision 5 Master Card and this section describes MAST Revision 2.2.

3.1 Timer Tests

Test name: TIM
No. tests: 4

Test No.1 "Master Timer Read/Write Latches"
Purpose: Check ability to communicate with timer.
The 3 timers in the 6840 timer AB6 are put into the preset state and all numbers from zero to $FFFF written to the timer latch. Each write is followed by a timer read for verification Timers 2 and 3 are then tested in the same way.
Each write/read is a double byte transfer through the 8-bit buss.

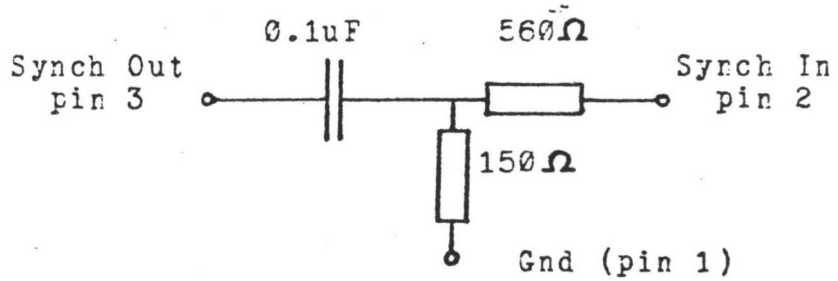
Test No.2 "Master Timer Internal Clock Timeout"
Purpose: Check timeout operation under internal clock.
The internal clock to the timer is ENB, from CAS. All thr timers are initialised to $FFFF then started. A software timi loop is used as reference, and the timer status is continual for premature timeout. Timeout must occur within a certain tolerance before or after reference timeout.
Clock outputs are enabled during the tests.

Test No.3 "Master Timer External Clock Timeout"
Purpose: Check timeout operation under external clock.
Timers are programmed as follows:-
Timer 2 Internal clock
Continuous operation
Initialised to 1
Output enabled

Timers 1&3 External clock (Timer 2 output)
Single shot
Initialised to $FFFF/2
Outputs enabled

The same reference is used to check that timers 1 and 3, being clocked by timer 2, times within tolerance.

Test No.4 "Master Synch In/Out"
Purpose: Checks click output and synch input circuits.
This is actually two tests run one after the other. Both require Synch In to be connected to Synch Out via an attenuator/filter circuit in order to load the output. (For in-house use on a complete CMI, this is contained inside a test plug which should be inserted in the SYNCH plug on the back panel). The circuit is illustrated below.



Synch Test Plug Circuit (3-pin Canon)

The first test clocks the Synch In timer (timer 2) with a k frequency and checks its timeout against the software reference. During initialisation, timer 1 is checked to be working (i.e. that it can be made to time out). It is then programmed for internal clock, and preset to run continuously at 250Hz with its output enabled. Timer 2 receives the sync input pulses and times out in single shot mode after 100 clocks (about 400mS). This timeout is verified against the software timer. Timer 3 is not used.
The second test sends a fixed number of pulses from timer to timer 2 and checks that timer 2 receives the correct number Timer 1 is set to internal clock and runs at 1000Ez. Timer 2 is initialised to $FFFF. The status register is polled for timer 1 timeouts and it is stoppped after 3000. Then timer 2's counter is read to check that it decremented to the correct number.

3.2 Master Pitch Register Test

Test name: PIT
No. tests: 1

Test No.1 "Master Pitch Register Test"
Purpose: Check for presence and accuracy of the master pitch reference signal MOSC.

This test requires a working channel card to be installed in the channel 1 slot. Each of the pitch rate multipliers (C1Ø, D1Ø) are tested separately by timing a number of segments and comparing it to a fixed value. The channel card is set at a fixed pitch, then the master pitch is preset through the PIA RC9, starting with the lowest pitch. Timer 3 on the channel card is used to time the segments. The EOSI flag is cleared on the channel card then RUN mode selected and the timer started. The channel status is polled for the arrival of EOSI and if it arrives outside a set tolerance from the timer 3 timeout, an error is gererated.

This cycle is repeated for all master pitch settings.

3.3 A-D Convertor System Tests

This section describes the MAST test version 2.2. This is a merged program containing tests using an external analog source from version 2.1 as well as tests using a channel card as an internal analog source from version 1.8. The AD, DI and DB commands of version 1.8 have been renamed ADI, DII and DBI respectively, while version 2.1 names are unchanged.

3.3.1 AD Tests using External Analog Source

These tests are designed for complete CMI's being tested with the Analog Tester Box.

Test name: AD
No. tests: 2
Purpose: Software check of A-D convertor system using a known analogue input.
Options: C=n Channel no.
Range 1-8, default 1
Channel 1 is always used, others may be specified.

Test No.1 "Analog to Digital Convertor 16kHz"

The Fairlight Analog Tester box provides a triangle wave of 10V p-p at 30Hz as a known input to the master card for sampling via the ADC switch on the back panel. The switch should be set to EXT ADC. Some cable rearrangements have to be made to use the tester:

(1) Keyboard Power cable, normally connected from the CMI to the Music Keyboard, should go to the analog tester.

(2) Alphanumeric keyboard, normally connected to the Music keyboard, should be connected directly to the CMI rear panel.

The analog tester brings out both sides of the balanced outputs from the channel cards. With the oscilloscope set on 1V/div, add CH1 and CH2 and trigger on CH1. Set the tester switches to SYNC and NORMAL.

The analog input is a triangle of a set frequency such that at the given sample rate (16kHz) the difference in consecutive samples is 0 or 1. The sample rate is initialised by loading a pitch into the pitch register of channel 1. This generates the buss signal ADCLK which is gated through to the AD571 by the non-assertion of ADM from the PIA.

A maximum allowable number of zero differences and a small number of "jumps of two" allowed are specified in the software. Non-zero differences should all be in the same direction for a rising or falling waveform.

Channel 1 and any other specified channels are set up to receive the converted data. Sampling starts, but no samples

are recorded in waveform memory until a zero byte is read, which must occur within a set timeout period (software timeout, doesn't use 6840 timer). Each sample is initiated by accessing $E026 (decoded as JAM) to reset D3. This halts processor 2 (running the test program) until the Data Ready signal (DR) from the AD convertor unjams the processor. D2 provides a hardware timeout in case the AD571 (D7) is not working at all.

Once a sufficient number of samples have been made and stored in channel 1 (& others if specified), sampling is stopped and the data in channel 1 read to check for a continuous rising waveform followed by a continuous falling one.

Test No.2 "Analog to Digital Convertor 30.2kHz"
This test is identical to test No. 1 except that a 30.2kHz sampling rate is used.

Test name: ADCHK
No. tests: 2
Purpose: AD conversion test for debugging.
Options: C=n Channel number
Range=1-8, default 1 (always used)
R=n Audtype
Range 0-2, default 0

Test No.1 "AD Run Continuous 16kHz"
Test No.2 "AD Run Continuous 30.2kHz"
These tests are the same as the AD tests except that sampling continues indefinitely to assist in debugging problems discovered by AD.

Test Name: DI
No. tests: 1
Purpose: AD conversion display.
Options: C=n Channel no.
Range 1-8, default 1

Test No.1 "Display Routine"
This simply sets up the specified channel to play back the sampled waveform last recorded by AD or ADCHK. Monitor it at TP6 or the mixed output. It should be a low frequency triangle. It is not necessary to do this except for debugging purposes as the software checks for the correct sampled data itself.

Test Name: DUMP
No. tests: 1
Purpose: For close examination of sampled data
Options: C=n Channel no.
Range 1-8, default 1
S=n Segment no.
Range 0-127, default 0

The contents of the specified channel and segment are printed on the screen in hexadecimal.

3.3.2 AD Tests Using Internal Analog Source

These tests are designed for the Torture Chamber and other test rigs, or a complete being tested without the Analog Tester box.

Test Name: ADI
No. tests: 2
Purpose: Tests A-D conversion system using a known analog input, generated from one of the channel cards.
Options: C=n Channel no.
Range 1-8, default 1
(Channel 1 always used, plus others as specified).
R=n Audio board type
Range Ø-2, default Ø

Test No.1 "Analog to Digital Convertor 16kHz"
Test No.2 "Analog to Digital Convertor 3Ø.2kHz"

Channel 1 must be available to provide the AD conversion clock to the master card. The other channels specified (or channel 1 by default) are loaded with a two-segment triangle wave to simulate the test waveform provided by the Analog Tester in the AD test.

On the test rigs, the B side of the channel 1 analog output is hard wired to the analog input on the audio board CMI-Ø4, which goes directly to the AD IN input of the master card. The Torture Chamber has a switch which selects either channel 1 or EXT (which is just ground) as the analog input: it should be at CH1 for the ADI test. Since only channel 1 is wired in this way the test won't work if it is not specified as a source channel.

If testing a complete CMI, connect the output of the channel to be used as the analog source to the EXT ADC input as below and set the ADC selector to EXT ADC.

	Pin		Pin	
GND	1		1	Ext ADC RTN
Side A	2		2	
Side B	3		3	Ext ADC IN
	CH_X_Socket		EXT_ADC_Socket	

The R option is to allow for the high gain of early version audio boards (prior to revision 4A.1). If it is desired to update an old board, refer to Field Change Notice 23.
The option determines the channel volume setting for playing the test waveform, as follows:

R=0 Test is first performed with volume setting for the old version audio board. The first conversion value is read and, if wrong, the volume is set for the lower gain new version audio board. The test is then repeated.

R=1 Test is performed with volume set for an old audio board only.

R=2 Test is performed with volume set for the new version audio board only.

Instead of storing the converted data in a channel card, it is written to a system RAM buffer. When 256 bytes have been read the values are checked as follows:

(1) All values must be increasing, but up to 2 successive values may be the same.
(2) There can be at most 1 missing code.

Test Name: DBI
No. Tests: 1
Purpose: Close examination of sampled data.

Test No.1 "Display Contents of Buffer"
Half of the contents of the 256-byte buffer in RAM, representing one side of the sampled waveform are printed on the screen.

Test Name: DII
No. Tests: 1
Purpose: Replay sampled waveform
OPtions: C=n Channel no.
Range 1-8, default 1

Test No.1 "Display Routine"
The contents of the RAM buffer are moved to the specified channel card memory and the channel set running until CNTRL ESC is typed. Monitor the waveform at TP6. It should be a low frequency triangle.
This test allows a quicker check of sampled data than DBI. Both display routines are only necessary for debugging as the ADI test itself checks if sampled data is correct.

Test Name: JAM
No. tests: 2

Test No.1 "P2 Jam and Unjam"
Purpose: Checks correct functioning of the processor 2 HALT circuit used by AD conversions.

The ADM signal from PIA DE5 is asserted so that the AD571 (IC D7) is clocked by DLE every time a the low order converted byte is read. The two processors execute synchronised code using some common data:

P1STD = flag to indicate processor 1 has started its part of the test code
CNT = counter which allows processor 1 to monitor processor 2's activity

The test proceeds as follows.

Processor 1	Processor 2
	Initialises and clears halt flag by accessing UNJAM Starts P1 Goes into loop which checks P1STD. If P1 doesn't start within timeout, gererates error and exits
Sets P1STD Short delay	
	Clears CNT Goes into loop incrementing CNT stays there until P1STD is cleared again
Halts P2 (JAM) Reads CNT Short delay Reads CNT again - if it has changed, P2 hasn't stopped Starts P2 (UNJAM) Short delay Reads CNT again - if it is the same P2 hasn't started again	
Clear P1STD	Tests error flags and terminates test

Test No.2 "P2 Jam Timeout"

Purpose: Tests the automatic processor 2 restart.

In the event of UNJAM never being accessed or a conversion never being completed, a hardware timeout is provided by one-shot D2 to restart P2. It must be possible to stop processor 2 for at least 200uS but no more than 1mS. The same common data is used as test No.1

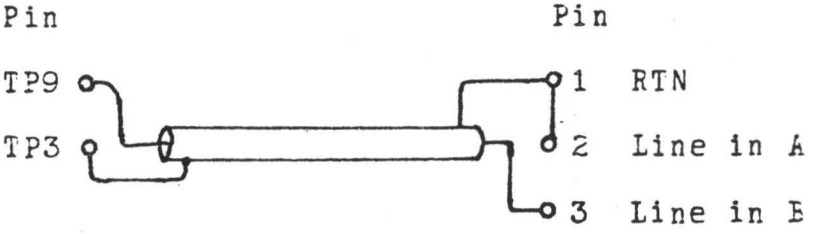
The test proceeds as follows:

Processor 1	Processor 2
	Initialises and clears halt flag by accessing UNJAM Starts P1 Goes into loop which checks P1STD. If P1 doesn't start within timeout, generates error and exits
Sets P1STD Short delay	Clears CNT Goes into loop incrementing CNT stays there until P1STD is cleared again
Halts P2 (JAM) Reads CNT Short delay Reads CNT again - if it is different, P2 hasn't stopped. Starts counting loop for up to 1mS, checking CNT to see if P2 has restarted automatically If timeout, UNJAM to try to restart P2 else, check loop counter to ensure P2 was stopped at least 200uS.	
Clear P1STD	Tests error flags and terminates test

3.4 Master Bandpass Filter Tests

Test Name: FILT
No. tests: 17
Purpose: Check characteristics of A-D convertor input filter.
Options: C=n Channel number
Range 1-8, default 8

The specified channel is set up to provide an analog test waveform. A special cable with a plug matching the row of channel card test pins is provided on the Torture Chamber and test rigs to take this signal from TP9, the unfiltered analog output, to the LINE IN input of the audio board and thence to the master card FIN input. If it is desired to replicate this on a complete CMI, connect as below and select LINE IN and INT ADC. Monitor the waveform at FILT OUT on the Torture Chamber or pin 3 of the SAMPLING FILTER OUT socket (pins 1 and 2 are GND).



CH X Test points LINE IN Socket

This test can also be performed using the Analog Tester box but the tester cannot gain access to the unfiltered channel output and uses the filtered output instead. This can indicate whether there is a major fault in the master filter but there is no point making accurate level measurements since the frequency responses of the channel card, master card, MIC or LINE input amplifiers and the tester itself are all superimposed. Set the tester to FILT OUT ONLY.

The upper nibbyl of the B side of PIA DE5 sets the high pass filter cutoff point while the lower nibbyl sets the low pass cutoff. The most significant bit of each nibbyl enables the corresponding filter multiplexors. Thus the PIA settings have the following effect:

$X8-XF	LPF at minimum cutoff frequency
$X0	LPF at maximum cutoff frequency
$0X	HPF at maximum cutoff frequency
$8X-FX	HPF at minimum cutoff frequency

Tests 1 to 9 fix the HPF at minimum cutoff while ranging the LPF from maximum to minimum respectively (0-8).
Tests 10-17 fix the LPF at maximum cutoff while ranging

the HPF from minimum to maximum (7-0). Step through the tests using the space bar.

All tests fill 4 segments of the specified channel with a fundamental sine wave, followed by another 4 segments of the 3rd harmonic. Channel pitch is set for each filter setting to obtain a predetermined attenuation ratio between the two frequencies. Timer 1 of the channel is set to loop around the 8 segments continuously and they are played through the analog bandpass filter at maximum vol and ramp settings.

Refer to Section 11 for expected waveforms.

High-pass Filter 3dB Point

The 3dB point of the Master Filter at the lowest setting of the high-pass filter should occur at less than 20Hz. This can be tested by typing

FILT,N=9<CR>

This sets the filter at $F8, which is the lowest setting of both high pass and low pass filters. Instead of using the channel card as analogue input as above, connect a signal generator to the LINE IN socket (if single-sided, use side B, pin 3). Set input selector to LINE IN. On the Torture Chamber or test rigs, feed into pin 16 of the audio board.

Monitor the master filter output at TP9 of the master card. With a line input of about 2.6V p-p at 500Hz, the filter output should peak at 10V p-p. Adjust frequency downwards until the filter output is 3dB down, i.e. 5V p-p. This frequency should be less than 20Hz.

Appendix 1 gives the filter characteristics for all settings.

3.5 Video Ram Control

Test name: RAM
No. tests: 2
Purpose: Check ability to map VRAM in and out of processor address space.

Test No.1 "RAM VRAM Uniqueness Alternate Write"
The 16k of video RAM can be used as system RAM by processor 2 by clearing CB2 of PIA BC9. This control is checked by first saving the contents of the screen (VRAM) in spare system RAM. Then the pattern $AA is written to $8000 (RAM), CB2 cleared to access VRAM, and the complement pattern ($55) written to VRAM $8000. This sequence is repeated for the entire 16k (with CB2 toggling after each write). Then the two blocks are alternately read from the beginning in the same way, to check for correct data in each block. Finally VRAM is restored to the original.

Test No.2 "RAM VRAM Uniqueness Alternate Read"
This is identical to test No.1 except that the pattern $55 is written to system RAM, and $AA to VRAM.

4.0 64K RAM Card Tests

4.1 MEMTST

A program for testing the 64K RAM card Q096 is MEMTST.CM which can be run by typing

MEMTST<CR>

with the CMI diagnostics disc in drive 0.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

The program usually resides in block 0 (lowest 16K block) so tests which involve overwriting this area move it somewhere else first and bring it back afterwards.

References:-

Drawings Q-096-00 to Q-096-04

Board component references apply to the Revision 4 RAM Card and this section describes MEMTST Revision 1.2.

Error messages will generally indicate the block where the error occurred. Block 0 is physically located on the Q-096 board in the eight RAM chips of row F - furthest away from the edge connector. Blocks 1-3 are rows E, D, and C respectively.

Test name: 29
No. tests: 9

Test No.1 "Mapram"
Purpose: This tests the ability to select blocks one at a time without contention or overwriting.

With the test program running in block 0, logical block 1 is mapped to physical block 1 (by writing the necessary data to mapram B3) and filled with 1's. Then logical block 1 is mapped to physical block 2 and filled with 2's. Similarly, physical block 3 is filled with 3's through logical block 1. That done, each physical block is selected in turn and read back for verification as logical block 1.

If no errors have occured, the contents of physical block 0 (including the program) are moved to physical block 3 and the test is repeated on blocks 0-2.

Test No.2 "P1 Odd Up, P2 Even Up",
Test No.3 "P1 Odd Down, P2 Even Up"
Test No.4 "P1 Odd Down, P2 Even Down"
Test No.5 "P1 Odd Up, P2 Even Down"
Test No.6 "P1 Odd, P2 Even"
Test No.7 "P1 Even, P2 Odd"
Test No.8 "P1 All"
Test No.9 "P2 All"
Purpose: Test the ability of both processors to write and read every location in RAM independently without interfering with each other.

Each processor starts with a given data pattern "seed" and adds 29 (decimal), modulo 255, each time it writes. This creates a discontinuous but exhaustive data sequence which can be reproduced for verification.

"P1 Odd" means that processor 1 writes and reads all odd locations only, while "P2 Even" means processor 2 writes/reads all even locations only, and so on. Thus the data from each processor is interleaved in memory.

"P1 Up" means that processor 1 starts writing to the bottom of memory (lowest address) and goes up. Once it reaches the top, a reading phase is entered to verify the data pattern from the top of memory back to the bottom. Conversely "P2 down" means processor 2 starts writing at the top and works down, then reads back from bottom to top.

"All" means the specified processor writes and reads both even and odd locations.

Tests 6-9 cause one or both processors as specified to start at both ends, writing to the top and bottom alternately and working in towards the middle. When the middle is reached the reading phase begins, reading from the middle, out towards the top and bottom.

Test name: WA
No. tests: 2
Purpose: More RAM mapping tests

Test No.1 "Walking Address P2"
Test No.2 "Walking Address P1"

These test the RAM mapping by writing a "walking address" to the location specified by that address, testing one block at a time. First the block is filled with pseudo-random data. Then, starting at the bottom of the block the high order 8 bits of the current address is written to an even location then read back for verification. The low order address byte is written in the next location and verified. This is continued to the end of the block (incrementing the address by two for each high-order/low order write). Then the whole block is read again for verification from the beginning.

Test name: MAP
No. tests: 4

Test No.1 "Map Uniqueness"

Purpose: This tests the ability to select blocks one at a time without contention or overwriting.

This test is effectively identical to "29" No.1

Test No.2 "Card Deselect"
Purpose: By mapping any logical block to a physical block greater than 3 it must be possible to deselect the entire RAM card.

The program runs in block Ø as usual. Blocks 1-3 are filled with data $55. Then logical block 1 is mapped to "physical" blocks 4 to 7 in turn, reading the whole block for $55's which should never come up. This establishes that deselected blocks cannot be read.

To check they can't be written to, $AA is written to logical block 1 then physical blocks 3, 2 and 1 are checked to still contain $55.

Test No.3 "Write Protect"
Purpose: Blocks can be selected for reading only

Physical blocks 1-3 are filled with $55 and verified. Then each of these blocks are mapped in turn to processor 2 block 1 with the write-enable bit removed. The write-enable bit is the least significant bit of the mapping byte written to the mapram. For each mapping, logical block 1 is cleared. Then all three physical blocks are checked to still contain $55.

Test No.4 "Map-Processor Uniqueness"
Purpose: Processors can be mapped independently.

Physical block 1 is mapped to processor 2 block 1, and physical block 2 is mapped to process or 1 block 1. Processor 1 fills its logical block 1 with 1's, and simultaneously, processor 2 fills its block 1 with 2's. Each processor then reads back its own block to verify for correct data.
N.B. - This test tends to cause the system to crash if the Q-Ø96 is on an extender card.

4.2 MEMCH

A handy program for testing faulty 64K RAM cards is MEMCH.CM. However a good board is required to load it in the first place. With a good Q-Ø96 in the appropriate slot, type

MEMCH<CR>

with the CMI diagnostices disc in drive Ø. The program loads to $FFØØ, which is processor-unique static RAM on the Debug card. Halt both processors, swap the faulty RAM card in, and release the processors.

The program writes a binary count, verifying after each write, to location $1ØØ of each block.

5.Ø Central Processor Control Module ("Debug Card")

Few diagnostics are available for testing the Debug card Q-Ø32 since it is not possible to load the DOS and run a test without most of the debug card functioning correctly.

5.1 User PIA and Real Time Clock

The user PIA and real time clock is tested by the program DEBTST.CM, which may be run by typing

DEBTST<CR>

with the CMI diagnostics disc in drive Ø.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

References:-

"CASAR Central Processor Module Functional Description"
Drawings QM8-026-ØØ to QM8-028-ØØ

Board component references apply to QØ32 version 3 only.

The PIA tests require a special test plug to be inserted in the user PIA socket (the one nearest the top of the board) which has the effect of connecting the A side of the PIA to the B side. Connections are as follows:

1 - 24, 2 - 25, 3 - 26,
5 - 22, 6 - 21, 7 - 20,
8 - 19, 9 - 18, 1Ø - 17,
11 - 16, 12 - 15.

Test Name: PIA
No. tests: 8

Test No.1 "PIA B/Send A/Receive"
Test No.2 "PIA A/Send B/Receive"
Purpose: With the test plug connecting the two sides of the PIA, A should be able to write to B and vice-versa.

Both tests check each side of the PIA individually first by defining the side as all bits inputs, changing them to outputs, then writing Ø, $FF, $FE etc. down to Ø again to the data register and reading back to verify each write.

Test no.1 then sets side A as all inputs and side B as all outputs and writes all values from Ø decrementing back to Ø to side B, AND reading from side A. Test no.2 does the same in the opposite direction.

Test No.3 "CB2/Send CA2/Receive -ve"
Test No.4 "CB2/Send CA2/Receive +ve"
Test No.5 "CA2/Send CB2/Receive -ve"
Test No.6 "CA2/Send CB2/Receive +ve"

Purpose: Interrupt inputs/control outputs check.

The signal specified by "Send CX2" is configured as a control output whose state is determined by CRB-3 in the PIA control register. The other signal is configured as an interrupt input which will set the interrupt flag in the control register on an edge whose direction is indicated by the "Receive +ve or -ve".

The transmit end is first set to the state which will allow the wrong transition to cause an interrupt, (i.e. if the interrupt receiver is +ve edge triggered, the transmit end is set high) and the flag is checked as clear. Then the transmit state is toggled and checked again as still clear. A second toggle should trigger the interrupt flag.

The actual IRQ output is disabled during the test.

Test No.7 "CA1: RTC Input 16.3mS"
Test No.8 "CB1: RTC Input 16.3mS"

Purpose: Real time clock and CA1/CB1 operation

Interrupt input CB1 is always connected to a real time clock signal (RTCB, from the refresh counter A5); inserting the test plug connects CA1 to it also.

During the test processor 1 is held in a tight loop to prevent it accidentally clearing the interrupt flag while processor 2 runs the test.

A long timeout loop is used first to check if the clock is working at all. The interrupt flag in the control reegister associated with CA1 or CB1 as specified is cleared then a polling loop entered to check if a new interrupt is received.

Immediately after the first "clock tick" is received, another counting/polling loop is entered to time when the next tick comes. When the second tick arrives the counter is checked to determine if clock is fast or slow. "Very slow" error message indicates that the most significant byte of the 16-bit counter was wrong.

6.Ø Light Pen Interface

References:-
Drawings QM8-148-ØØ to QM8-148-02

Board component references apply to Light Pen Interface version 3 only.

6.1 CMILP

A quick check of the functions of the Light Pen Interface card Q-148 is provided by the program CMILP.CM which may be run by typing

CMILP<CR>

with the CMI diagnostics disc in drive Ø. This test does not use the standard command interpreter.

The commands to CMILP are very simple:

I - Invert entire screen
C - Clear entire screen
Q - Quit

Just type the letter to initiate a command.

With the screen all "white" it should be possible to see the cursor field when the tip of the light pen is not touched, and draw single-dot "black" lines on the screen when it is touched. With the monitor adjusted to normal brightness the light pen sensitivity (a small screw under the rubber cap on the light pen body) should be adjusted so that the cursor is as small as possible but still distinct.

Check that it is possible to draw anywhere on the screen except the top two rows and the left most 8 columns. Try inverting the screen.

6.2 LPTST

For more careful diagnosis of a faulty board, use LPTST.CM run by typing

LPTST<CR>

with the CMI diagnostics disc in drive Ø.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<CR>

This section describes LPTST Version 1.3

6.2.1 Light Pen Timers

Test name: TIM
No. tests: 4

Test No.1 "Light Pen Timer Read/Write Latches"
Purpose: 6840 timer preset latches can be written to and the counters read.

Timers are put into preset state in which the counters always reflect the contents of the preset latches. Then each timer is write/read tested with all numbers from 0 to $FFFF. Each write/read is a 16-bit transfer through the 8-bit buss.

Test No. 2 "Light Pen Timer Internal Clock Timeout"
Purpose: Correct timeout from timers under internal clock

The internal clock is provided by the BCA signal. Timer outputs are enabled and latches preset to $FFFF. Then all three counters are released and their timecuts compared to a software status-polling (to sense timeout) timing reference loop.

Test No.3 "Light Pen Timer 2 External Clock"
Test No.4 "Light Pen Timer 3 External Clock"
Purpose: Timers under external clock

Timer 2 counts frames, thus gets a 20mS clock cycle. The test is not synchronised to the frame pulses so a +/-10mS jitter is permissible. The timer is preset to count 200 clocks (4 secs), then released and compared to the software reference with the required tolerance.

Timer 3 is clocked by processor 2 phase 2 (1MHz). It is preset to $FFFF then released and its timeout compared to the software reference.

Both timers run in single shot mode with outputs enabled.

6.2.2 Light Pen PIA

Test name: PIA
No. tests: 1

Test No.1 "PIA Test"
Purpose: You've got 3 guesses

Each side of the PIA is configured as all outputs then all numbers from zero backwards down to zero are written to the data latches and verified.

6.2.3 Processor Access Selection

"Test" name: SEL
Purpose: Allows user to specify which processor can access the video RAM.
Options C=n CPU selection
Range 1-2, default 2

All CMI's allow Processor 2 only to access the VRAM. By default, this processor runs the LPEN test but to use this test on a QASAR G, (whose Processor 1 accesses VRAM only), call SEL,C=1 to swap processors.

Typing SEL without any C option results in a report of which processor has been selected but makes no change.

6.2.4 Light Pen Drawing

Test name: LPEN
No. tests: 1

Test No.1 "Light Pen Drawing on Screen"
Purpose: Overall light pen operation, similar to CMILP.
Options: L=1 Range Ø-1, default 1
1 causes hit addresses to be written on the screen

S=s Range Ø-1, default 1
Ø inhibits resetting of the scroll reg.

Use LPEN the same way as CMILP. With hit address writing enabled, the location of each hit is written on the bottom line of the screen, both as X,Y coordianates and as an address in video ram. The line number is given first (zero at the top) followed by two bytes representing the location of the hit on that line. The first byte should always be Ø or 1 and represents the least significant bit of the 9-bit location (512 dots per line). The second byte is the upper 8 bits of the location. The VRAM ADRS is the absolute address of the hit in video RAM and is followed by a byte indicating which bit of that address was hit.

7.0 Graphics System

A functional check of the Graphics Controller Q-045 and 16K Graphics RAM Q-025 can be run by typing

GRAPH3<CR>

with the CMI diagnostics disc in drive 0. This test doesn't use the standard command interpreter.

GRAPH3 does not test the Q-025 directly as MEMTST tests the Q-096 memory. However, graphics RAM faults will generally be apparent from the screen display. An software test of the Q-025, though not exhaustive is the RAM VRAM Uniqueness tests in MAST (see section 3.5).

References:-

Drawings Q045 (4 sheets)
and QM8 025-01 to QM8 025-02

Board component references apply to Q-045 version 3 only.

Graph3 Commands:-

A single hex digit 0-B calls one of 11 simple graphics drawing functions. Each command begins in the centre of the screen and draws out in the specified direction to the edge and wraps back around to the centre. Drawing may be started and stopped, speeded up and slowed down as below:

Type	Effect
1	Horizontal line to the right
2	Horizontal line to the left
3	Single horizontal byte at the centre
4	Vertical line downwards (single dot, pattern $80)
5	45 degree diagonal down to the right
6	45 degree diagonal down to the left
7	Heavy vertical column downwards (1 byte wide, pattern $FF)
8	Vertical line upwards, single dot wide
9	45 degree diagonal up to right
A	45 degree diagonal up to left
B	Heavy vertical column upwards ($FF)
S	Slower speed
I	Increase speed
P	Change write pattern
H	Halt
C	Clear screen
G	Go

All drawing is done a byte at a time and except for command 3 which only writes a single byte, consists of writing repetitively to the appropriate Q-045 auto increment/decrement

register. The Q-045 specification sheet contains a list of which locations perform these automatic functions. By default, the drawing "pattern" is $FF so that all lines are unbroken. By using the P command the drawing pattern can be used to create broken lines. This is handy for finding single-bit errors (usually originating on the RAM card). The vertical line commands 4 and 8 mask off all but the most significant bit so any pattern without this bit won't draw anything for those commands.

GRAPH3 should be used to check the location of video information between the horizontal synch pulses. This can be controlled by the two trimpots at the front of the Q-045 board. RV2 (upper trimpot) sets the horizontal width, and RV1 (lower) sets the horizontal position. Adjust these using the double diamond pattern formed by commands 5 and 6 or 9 and A. The pattern should be symmetrical and just touch the edges of the active video area of the screen.

8.Ø Floppy Disc Controller

As is the case for the Debug board, nothing much can run if the floppy disc controller doesn't work. However there are two little programs described here which, once loaded using a good floppy controller, can be of some use in debugging the faulty QFC-2 board.

References:-

"Floppy Disk Controller/Formatter QFC2"
Drawings QFC2-Ø to QFC2-4
"CASAR Diskette System Maintainance"

The last document gives useful information for determining whether a fault is due to the controller, the disc drive, or a corrupted disc. It also provides disc drive set up and alignment information.

Board component references apply to the Revision 3 Floppy Disc Controller.

8.1 FDCFIX

The program FDCFIX.CM is loaded by typing

FDCFIX<CR>

with the diagnostics disc in drive Ø and a working QFC-2 installed. This loads the program to $9FEE and exits immediately back to the operating system. Halt both processors, and swap in the faulty board but DO NOT connect the 50-way ribbon cable to the disc drives. Release the processors and press the console interrupt to enter the monitor. Type

A000;G

to run the program (no <CR> required, and no message is printed to indicate the program is running).
All it does is loop around, alternately writing and reading the D status registers at $FCE0 to $FCE7. No verification is performed.

8.2 FDCDMA

The program FDCDMA.CM is loaded by typing

FDCDMA<CR>

with the diagnostics disc in drive Ø and a working floppy controller installed. It loads to around $A100 but immediately exits back to QDOS without running.

Its function is to exercise the DMA logic. To get a DRQ signal on the faulty board, remove the floppy controller chip and insert a link between pins 38 and 2 of the socket (for in-house use, there is a dummy chip for this purpose).Halt

the processors and swap the faulty board in but DO NOT connect the 50-way ribbon to the disc drives. Press console interrupt to enter the monitor and type

```
A102;G
```

to jump to the program (no <CR> is required, and no message is generated to indicate the program is running). The program is simply a little loop which writes $04 to the DMA register at $FCE6 indicating a DMA read command, then writes $05 (any number would do) to $FCE0 to generate a WE signal and hence a DRQ. Note that this does not test the DRQ under a write command.

8.3 QFC-2 Alignment

Adustment of two separate pulse lengths is required in the data separator section of the floppy disc controller. The test signals are available at points TP1 and TP2 and adjusted by 10-turn pots VR1 and VR2 respectively, on the QFC-2 board.

With a CRO set to .5uS/div and positive triggered, both signals should be high for 2.7uS when no data is being read from the disc (TP1 gets reset earlier by data pulses when the disc is being read).

9.0 Interrupt Tests - CMIINT

CMIINT.CM is a program for testing all the interrupt mechanisms in a complete CMI. It is run by typing

CMIINT<CR>

with the CMI diagnostics disc in drive 0. It does not use the standard command interpreter but has its own commands to set up and run interrupt tests.

Each interrupt has a predetermined priority such that if two or more interrupts arrived since the last interrupt service, the one with the highest priority gets serviced first. This arbitration is carried out by three Programmable Interrupt Control Units (PICU's): IC A10 and IC C10 on the Debug board Q032 and IC A6 on the Master Card CMI-02. Operating in tandem (all the interrupts handled by one PICU have a higher priority than those handled by the next), the PICU's determine which is the highest priority interrupt pending at any time, and generate an interrupt vector appropriate for that interrupt.
For further information on the interrupt arbitration, refer to:

"QASAR Central Processor Module Functional Description"
Drawings QM8-026-00 to QM8-028-00
"CMI-02 Master Card Functional Description"
Drawings CMI-02-01 to CMI-02-04

The "level" of an interrupt is a number indicating its priority such that the highest priority interrupts have a level of zero, and the others are arranged in ascending order of level for decreasing priority. The interrupts which may be tested by CMIINT, the part of the system from which they originate, their levels and the processor which services each one, are as follows:

Name	Origin	Level	Processor
CHANNEL 1	Channel 1 timer	12	1
CHANNEL 2	Channel 2 timer	8	1
CHANNEL 3	Channel 3 timer	13	1
CHANNEL 4	Channel 4 timer	9	1
CHANNEL 5	Channel 5 timer	14	1
CHANNEL 6	Channel 6 timer	10	1
CHANNEL 7	Chennel 7 timer	15	1
CHANNEL 8	Channel 8 timer	11	1
TIMER 1	Master Card timer	1	1
ACIA 1	Debug Card ACIA	0	1
TICKL 1	Interprocessor intrpt	2	1
TICKL 2	Interprocessor intrpt	2	2
TIMER 2	Light pen timer	1	2
DISK 1	Floppy disc controller	0	2

CMIINT Commands

RUN — Run tests on all active interrupts. Both sequential test (one interrupt at a time) and simultaneous test (triggered simultaneously, arrival checked for correct priority) will be run unless the SEQ or SIM commands have been used (see below). Run will be aborted if error count is exceeded or if the user hits CNTRL ESC (break).

REPEAT n — Sets the repeat count to n. The original value is printed. A repeat count of zero will continue indefinitely until aborted.

ERROR n — Sets maximum error count for RUN. Default is 1.

CMDS — Print a list of available commands.

LIST — List all interrupts and their statuses.

HELP — Print a summary of how to use the test

QU — Return to QDOS

+ <interrupt or function>
Activate an interrupt or function

- <interrupt or function>
Deactivate an interrupt or function

The interrupts which may be activated or deactivated using the + or - commands are as in the above list: just type "+" or "-" followed by the interrupt name. The "+" is always optional, and the name by itself will activate that interrupt or function. The functions which may be controlled in this way are:

P1	Testing of all processor 1 interrupts
P2	Testing of all processor 2 interrupts
ALL	(De)Activate all interrupts
LEVEL n	(De)Activate all interrupts of level n
SEQ	Sequential testing
SIM	Simultaneous testing
EMSG	Generation of error messages
DISPLAY	Listing of recorded interrupts on screen

General Procedure of Tests

Initially, all interrupts are "active", i.e., will be tested upon typing the RUN command. Tests can be activated or deactivated using the commands above. Each test begins with the processor interrupt mask set so that interrupts currently pending are ignored. The status registers associated with each active interrupt is read in order to clear pending interrupts. These status registers generally contain a flag which indicates an interrupt has been generated and at this point the flag should be clear.
All active interrupts are tested first sequentially (one at a time) then simultaneously. In the latter case, all active tests are "triggered" then the processor interrupt mask cleared. A delay loop sufficiently long for all triggered interrupts to arrive is entered. The PICU's should continue to interrupt the processors with the currently highest interrupt pending until all have been serviced. A separate service routine is executed for each interrupt which records in a little block of data set aside for each one, its position in the sequence of interrupts when it actually arrived, whether that interrupt has been serviced before, and whether the interrupt flag in the associated status register is set. Then the flag is cleared.

At the completion of the delay loop the data blocks of each interrupt is checked to ensure the active ones arrived in the correct order and that no unexpected interrupts occurred.

Note that interrupt vectors set up by the PICU's are multiplexed on to the address buss by latches E6 and E8 and buffers C3, C4, D3, and D4 on the Debug Card. If this mechanism does not work, or if the PICU's have not been programmed successfully, the system will undoubtedly crash when one of the processors attempts to jump to the interrupt service routine.

Error Messages

If error reporting has not been suppressed by a "-EMSG" command, messages will be generated indicating the error type and the interrupt test which generated it. The types of errors detected are as follows:

(1) "High Priority Interrupt Occurred Too Late"
Generated when the interrupt just received has a priority level less than the maximum found so far.

(2) "Interrupt Late ? Due to Previous Error"
One or more interrupts may appear to be late when they actually occurred at the right time, but a previous high-level (low priority) interrupt was too early and set an erroneously high current maximum level. The early low priority interrupt will not have been detected.
This message is generated when the interrupt just received is consistent with the immediately preceeding interrupt (i.e. has a greater level) but has a lower level than

the current maximum. Refer to the diagram on the following page for a clearer explanation of this problem.

(3) "Missing Interrupt"
An interrupt wich was expected never arrived

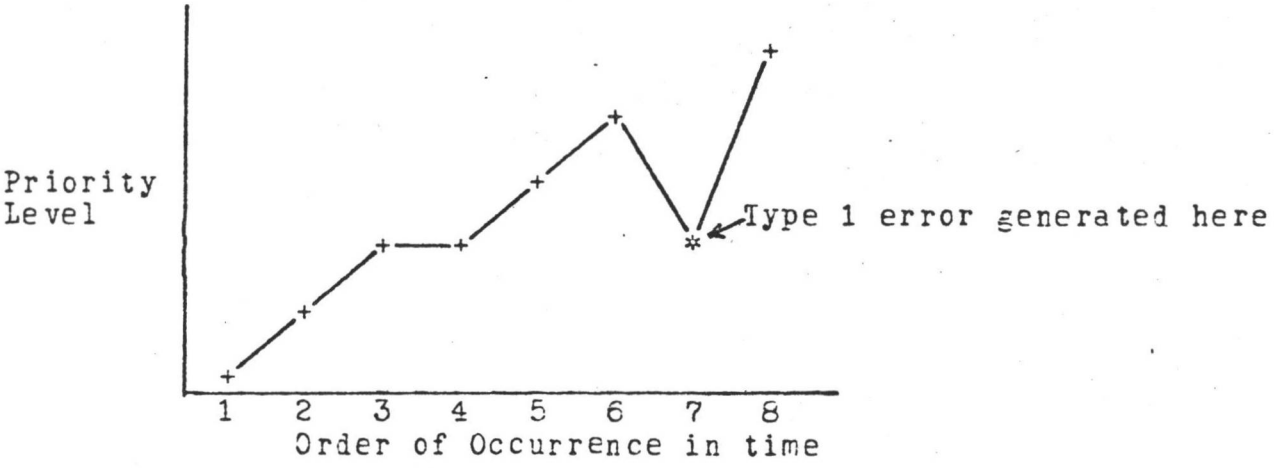
(4) "Multiple Interrupt"
An interrupt appeared to occur more than once. Usually caused by the interrupt not being cleared successfully by the service routine.

(5) "Unexpected Interrupt"
An inactive interrupt occurred.

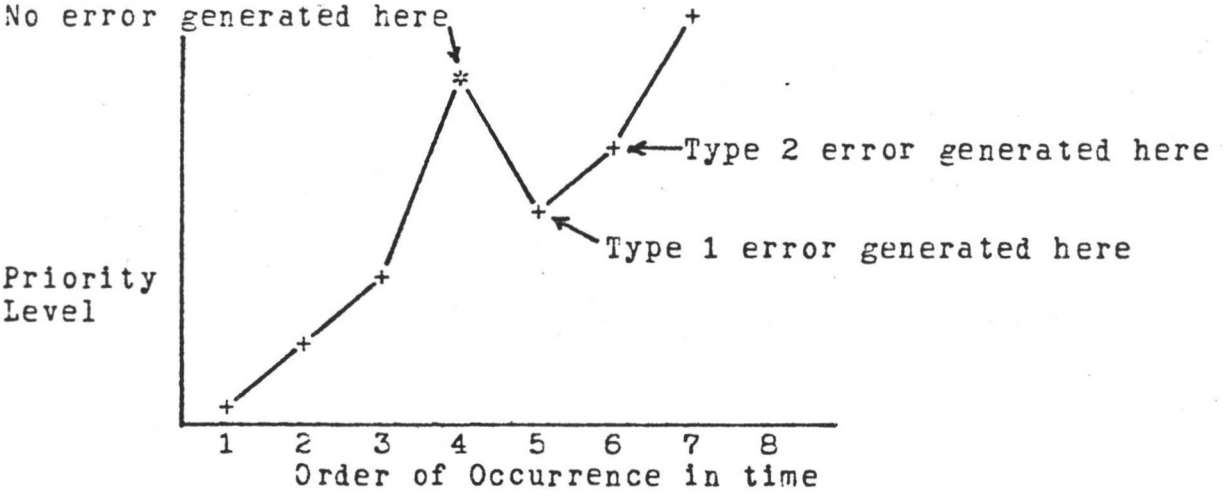
(6) "Flag Not Set"
The service routine found that its associated interrupt flag had not been raised.

Diagrammatic Representation of Interrupt Priority Errors

Key
+ interrupt in correct order
* interrupt out of order



(1) Correct detection of a high priority interrupt arriving too late



(2) Incorrect error detection due to early low priority interrupt.

Early interrupt is not detected because it is the lowest priority interrupt received so far.

10.0 Testing a Complete CMI - Chain Tests

The CHAIN command is a QDOS facility which allows many tests such as those described above to be run with the minimum amount of human intervention. The general form of a CHAIN command is

CHAIN <chain file>[:1];[<option1>,<option2>...]<CR>

where chain files are things with the suffix ".CF" .
The ":1" means the chain file is on drive 1, not Ø.
This section is a description of the standard chain files used for testing a complete CMI. Further information about the CHAIN command and how to write your own chain files can be found in the QDOS User's Guide.

10.1 Digital System Tests

Chain test name: CMITEST or CMITEST1
Purpose : All functions of a CMI which can be tested directly under software control (i.e. no waveform observations required)

CMITEST1 is for systems with only 1 disc drive and omits tests requiring 2 drives. CMITEST requires a scratch or another diagnostics disc in drive 1.

Test progs run	Commands executed
CMIINT	-DISK, RUN
DEBTST	All commands
CMITST	MEM, PIT, FLG, TIM
MEMTST	All commands
LPTST	PIA, TIM
MAST	PIT, RAM, JAM, TIM, AD

Also - BACKUP (CMITEST only)
CHECK;V
COPY (drive Ø to drive 1 in CMITEST, Ø to Ø in CMITEST1)

Options:

C=n	Channels to be tested. Default is 1-8
-T	Omit timer (TIM) test in MAST
-MAST	Omit MAST altogther
AD	Include A-D conversion tests in MAST

Test runs continuously.

10.2 Channel Card Analogue Tests

Chain test name: FRV
Purpose: Analogue functions of channel cards.

Test progs run	Commands Executed
CMITST only	FILT, RAMP, VOL

Options: none

All channels are tested. Step through the tests with a press of the space bar. FILT, RAMP and VOL are called on each channel individually, then FILT N=1 is called repetitively starting with channel 1 and adding another channel each time the space bar is pressed. This tests the mixer on the audio card in the back of the CMI. The amplitude should increase each time another channel is mixed in.

10.3 Comprehensive Analogue Test

Chain test name: ANALOG
To check: all analog functions of the CMI channel cards, master card, and audio card.

Test progs run	Commands executed
CMITST	RAMP, FILT, VOL
MAST	FILT, SYNC, AD.

Options:
M Omit channel card tests

This test is most conveniently used with the Analog Tester box connected to the rear panel of the CMI as labelled. Some cables need to be arranged slightly differently from normal. To make the changes, eject the disc(s), and turn power off first.
(1) Keyboard Power cable, normally connected from the CMI to the Music Keyboard, should go to the analog tester.
(2) Alphanumeric keyboard, normally connected to the Music keyboard, should be connected directly to the CMI rear panel.

The test program gives operator prompts and is thus largely self-explanatory. The following is some background on the use and functions of the analog tester.

Connection to CRO

The analog tester brings out both sides of the balanced outputs from the channel cards. With the oscilloscope set on 1V/div, add CH1 and CH2 and trigger on CH1.

The chain tests call standard tests described in previous sections which specify waveform measurements at TP6 of the channel card. This is only one side of the balanced output so measurements made using the analog tester will be about twice the amplitude found on TP6. For example in CMITST test FILT, the low frequency amplitude should be 6.8V p-p.

Switch 1 Phase Position

The phase check is to ensure that the different channels are in phase with each other.

Switch 1 Normal Position

This provides the balanced outputs to the CRO as above.

Mixed Out Test

This is the same as used in the FRV chain tests where FILT,N=1 is called repetitively starting with channel 1 only and mixing another channel in with each press of the space bar. The amplitude should increase with each new channel, reaching a maximum of 6.8V p-p. This tests the audio mixer board in the

back of the CMI.

MIC/LINE switching in MASTer test

By means of software and the analog tester, the output of channel 2 is fed to the MIC and LINE inputs and one or the other is fed to the Master card via the MIC/LINE switch. Although these two levels are actually quite different, the signals from the analog tester are similar in magnitude but still distinguishable. A sinusoidal waveform followed by a heavily attenuated harmonic should be observed with a peak amplitude of 1.5V p-p for MIC and 1.3V p-p for LINE.

The SYNC test

No measurement is required: the software will inform you of a fault although there is a filtered square wave which can be observed and an audible tone whose volume can be controlled by the SYNC MONITOR pot.

AD Test

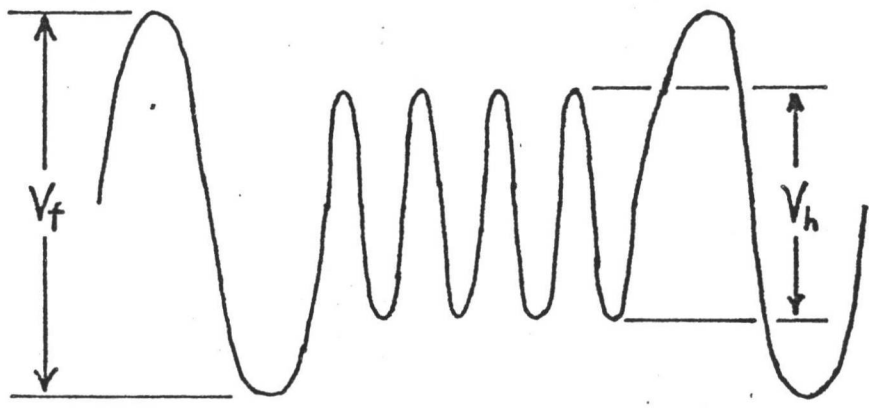
This is also a software test only

11.0 Summary of Test Waveforms

Measurement tolerances: refer to the introduction
(TP6) means measured at Test Point 6 of the Channel Card under test.
(AT) means measured using the Analog Tester, adding CRO channels.

11.1 CMITST

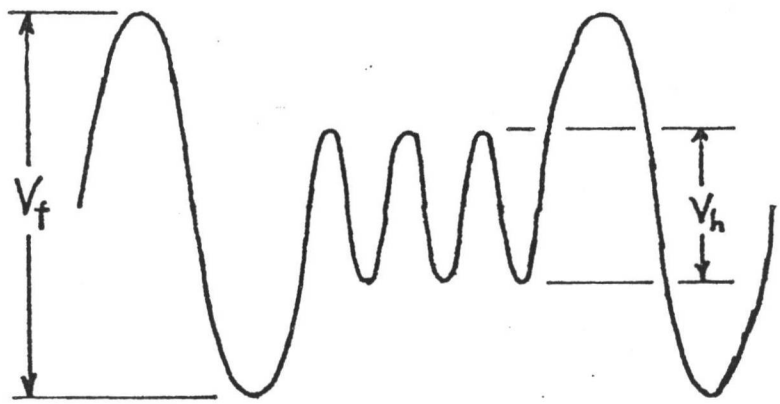
FILT



Vf = 3.4V p-p (TP6) for all tests
6.8V p-p (AT)

Test N	1	2	3	4-6	7-15
Vh, V p-p (TP6)	2.2	1.6	1.3	1.1	1.2
Vh, V p-p (AT)	4	3.5	3.3	3.0	3.2

FILTD

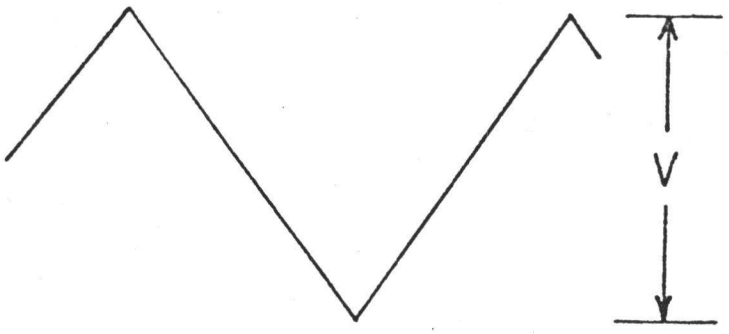


Levels depend on harmonic and filter settings. Levels for FILTD with default settings are as follows:

Test N	1	2	3
Vf, V p-p (TP6)	3.6	4.0	4.5
Vh, V p-p (TP6)	4.5	<0.2	<0.1

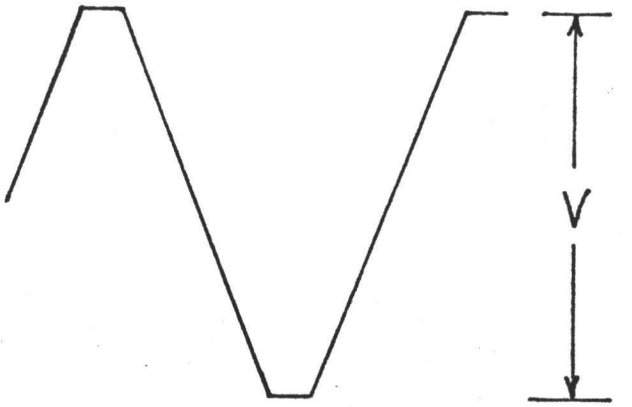
("<" = less than)

RAMP, N=1 "Ramp Preset"



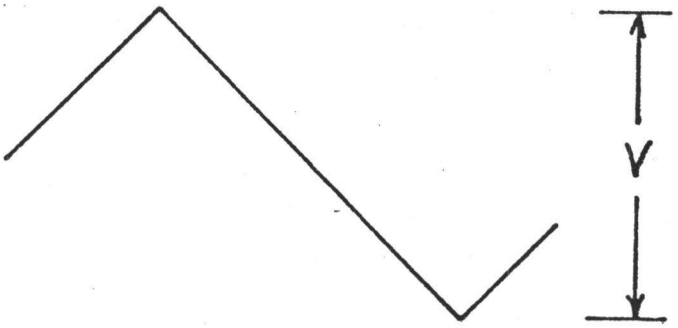
V = 2V p-p (TP6)
4V p-p (AT)

RAMP, N=2 "Ramp Auto Run"
N=3 "Force Ramp Up and Down"



V = 2V p-p (TP6)
4V p-p (AT)

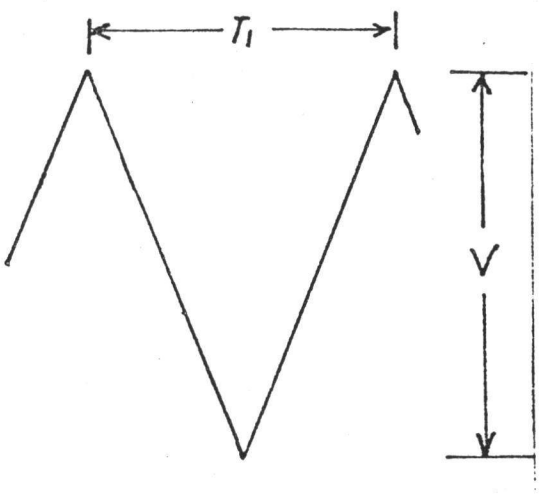
VOL, N=1 "Master Volume"



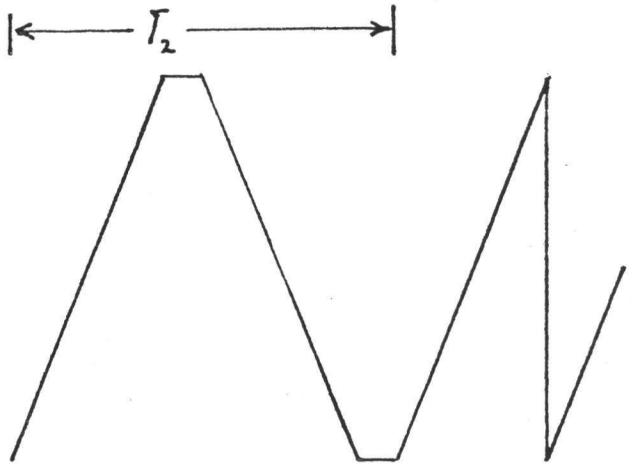
V = 2V p-p (TP6)
4V p-p (AT)

11.2 MAST

AD



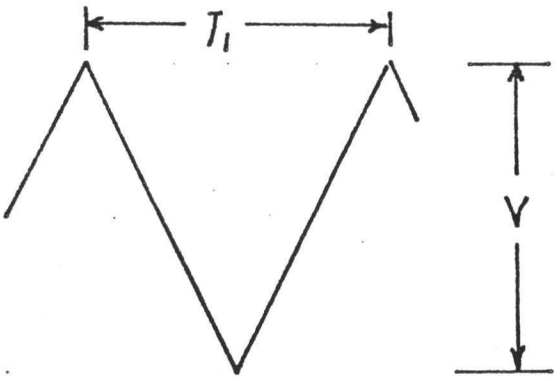
DI



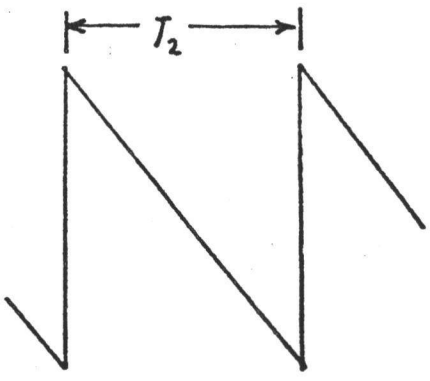
V = 8V p-p (AT)

	T1 mS	T2 mS
N=1	30	18
N=2	17.5	12

ADI, ADCHK



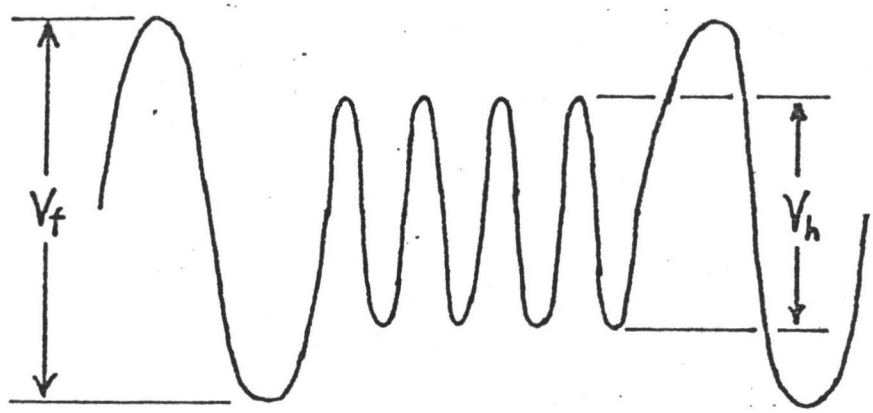
DII



V = 2V p-p (TP6)

	T1 mS	T2 mS
N=1	30	4
N=2	17.5	4

FILT



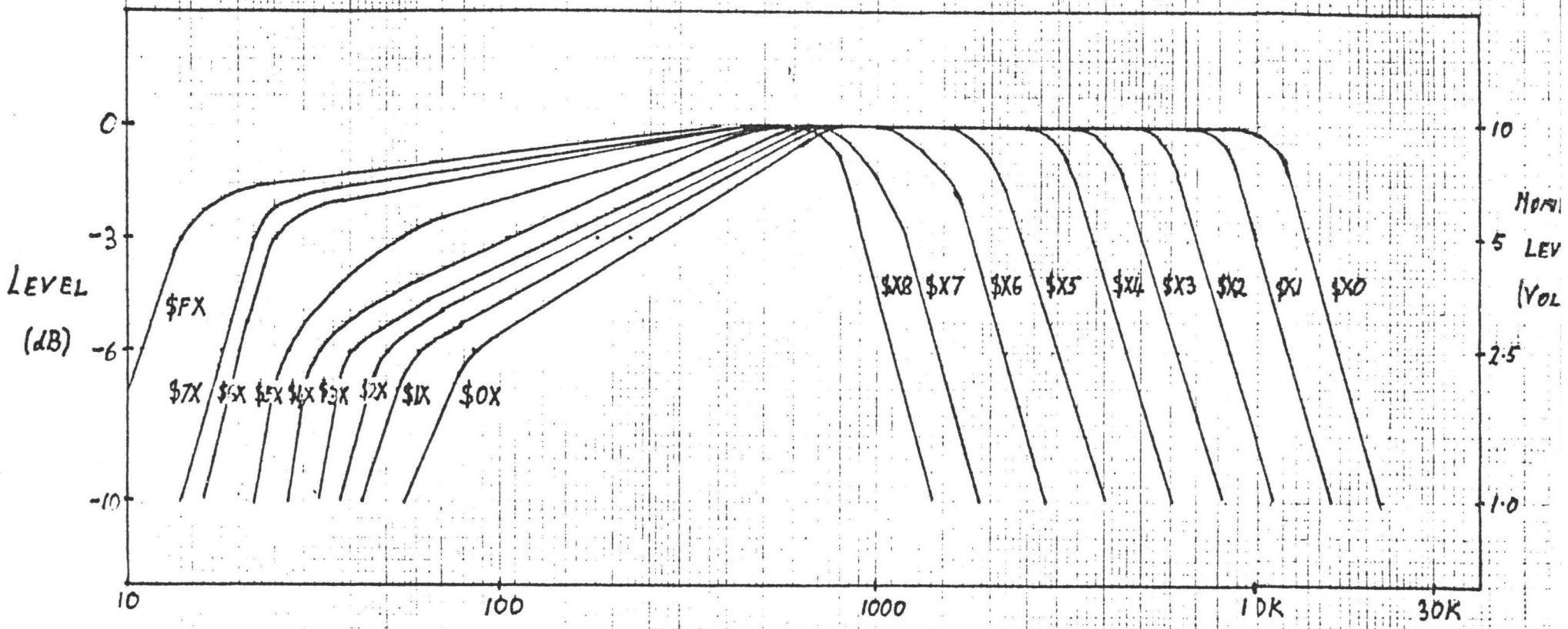
For N=1:
Vf = 4V p-p at FILT OUT on Torture Chamber
1.5V p-p for AT with CMI switched to MIC IN
1.3V p-p for AT " " " " LINE IN

N= 1 to 17, Torture Chamber:

Test N	1	2-5	6-7	8-10	11-17
Vf, V p-p	4	3.8	3.4	3.2	1.5
Vh, V p-p	2	2.2	2	2	3

APPENDIX

MASTER CARD BANDPASS FILTER CHARACTERISTICS



NOTE: $NN means hexadecimal notation for filter setting

X means "don't care"

QASAR

DISKETTE SYSTEM

MAINTENANCE

(1) QFC-2 Floppy disc controller alignment

(2) YD-174 Disc drive set-up and alignment

(3) Disc system fault diagnosis

FAIRLIGHT INSTRUMENTS

September 1981

DISC SYSTEM SET-UP AND DIAGNOSIS

(1) QFC-2 Floppy disc controller alignment
(2) YD-174 Disc drive set-up and alignment
(3) Disc system diagnosis

1) QFC-2 Alignment

Adustment of two separate pulse lengths is required in the data separator section of the floppy disc controller. The test signals are available at points TP1 and TP2 and adjusted by 10-turn pots VR1 and VR2 respectively, on the QFC-2 board.

With a CRO set to .5uS/div and positive triggered, both signals should be high for 2.7uS when no data is being read from the disc (TP1 gets reset by data pulses).

2) YD-174 Disc Drive Pre-alignment Set-up

(1) Check that 115V motor is fitted

(2) Check that 50Hz pulley is fitted

(3) Link 'Y' on YE Data p.c.b.

(4) Link 'C' on " " " .

(5) Move link to DS2 on p.c.b.

(6) Remove link block package and open circuit links 'X' and 'Z' (break legs off link block package)

(7) Reinstall link block

Disc Drive Alignment

New disc drives require the radial alignment to be checked.

(1) Place the drive on its side, with the main drive motor towards the bottom.

(2) Connect a CRO as follows to the block of test pins marked "TP" near the centre of the YE Data p.c.b.

Pin	CRO
A	Channel A
B	Channel B
3	Ext trig

(3) Set the CRO as follows:
Inputs on AC
trig on external negative
time base to 20 mS/div
add channels A and B
invert one channel
vertical sensitivity to 100mV/div

(4) Load a disc containing the test program DSKTST and run it by typing DSKTST<CR>.

(5) Type
RA,D,S<CR> where D = drive number (0 or 1)
S = side number (0 or 1)

(6) Insert Alignment Disc and hit a key. This steps the head to track 38.

(7) A "double eye" pattern should appear on the CRO. The amplitudes of the two lobes must be within 70% of each other.

(8) If side 0 is acceptable, repeat test for side 1

(9) If either side requires adjustment, loosen the two Phillips head screws which clamp the head carriage assembly to the steel stepper motor belt. The screws are accessed through two holes in the side of the drive chassis.

(10) Gently tap the carriage assembly or move the belt by hand until the lobes are within 70% amplitude with the screws retightened (tightening the screws tends to change the lobe pattern), for both sides of the disc.

(11) Hit ESC to terminate the radial alignment test.

Track Zero Sensor Test

After the head is radially aligned, the track 00 sensor should be checked.

(1) Still running DSKTST, type
T0,D where D = drive (0 or 1)

(2) Insert a scratch disc and hit any key.

(3) T0 causes the head to oscillate between track 00 and track 01. Monitor the sensor signal at pin B12 of the J2 connector block on the drive p.c.b. It should oscillate with movement of the head.

(4) Terminate test by hitting ESC

3) Disc System Diagnosis

The general procedure to follow in disc system fault tracing is:

(1) Use the system test program CHECK to determine if the fault is in the drive itself (or the diskette) or the disc controller/DMA data transfer system.

(2) If the disc drive is faulty, use DSKTST to further analyse the fault.

Test Program CHECK

Allows checking of

- Cyclic Redundancy Check (CRC) errors
- Data transfer between memory and disc
- RAM bit corruption errors

Command Syntax

CHECK <UNIT>,<HEXNUM>;<OPTIONS>

<UNIT>::=<COLON><NUMBER>

<HEX NUMBER>::=<HEX DIGIT>|<HEX DIGIT>

<HEX DIGIT>::=<NUMBER>|A|B|C|D|E|F

<NUMBER>::=1|2|3|4|5|6|7|8|9|0

(1) Disc Integrity Check

Options: none required

This is the default check routine. Entire disc in specified drive is read to check for CRC errors.

(2) Read Data D.M.A. Verify

Option: V

Reads entire disc in specified drive twice, into separate blocks of memory and verifies data against itself.

(3) Write Data D.M.A. Verify

Options: W,D (May be used together)

The W option creates a file, writes distinctive data to each sector of the file and reads each sector of the file back, twice, into different areas of memory for verification. All unfree disc space will be allocated to the file.

The D option is a destructive (to the disc contents) test which writes a unique "ADD -29" pattern to each sector in an interleaved fashion, reads it back, and verifies the data.

Interleaving of blocks ensures track boundaries are continually being crossed. A delay can be introduced using the "T" option (see below) to isolate head-load timing problems.

(4) Other Options

Option	Use with	
R	W	use random number pattern instead of "29" pattern
P=XX	W	use pattern XX where XX = 'hex number' write the pattern to disk, read back and verify
E=XX	all	print error if total recoverable disc errors exceed XX where XX = 'hex number'. D Default value is 0.
T=XX	all	delay XX*10 ms. after a read/write where XX = 'hex number'
C	all	test continuously alternating between 'add-29' and a random number pattern
L	all	all error messages printed on printer

(5) Error messages

(a) Disc Read/Write Errors
These are of the form

**PROM I/O ERROR -- STATUS = 'status byte' AT h DRIVE i - PSN j

where h is not significant
i = drive number
j = physical sector number at which the error occurred
and the status byte can be interpreted as follows:

31 data C.R.C. error
32 disk is write protected
33 disk is not ready for some reason
34 deleted data address mark read
35 abnormal command termination

36 invalid sector address
37 seek error (track not found)
38 data mark read error
39 address mark read error

(b) Verify Errors

When a verify error is encountered the offending disc sector is re-read into the QDOS sector buffer and matched against system RAM to determine where the error came from. The program then reports the corresponding address in RAM, the data expected, the erroneous data, the physical sector number of the disc where the error occured, and the byte offset within the sector.

(6) Termination

Test is terminated by -

3SC key (sets system error status word)
More then 20 errors logged
User supplied iteration counter expired (default 1)

System error status word will be set if any error condition has been reported.

Test Program DSKTST

DSKTST comprises five main test routines and a number of utility commands. The main routines are as follows -

```
#1 Write/read test                (destructive)
#2 Read C.R.C. test               (non-destructive)
#3 Worst case seek test           (non-destructive)
#4 Worst case data pattern R/W    (destructive)
#5 Sector/drive uniqueness        (destructive)
```

Tests can be run separately or in destructive/non-destruct groups by typing as follows -

```
DN,(0 or 1 or B) [,X]<CR>  (Do all non-destruct tests)
DD,(0 or 1 or B) [,X]<CR>  (Do all destructive tests)
ST#(up to 10 test no's separated by (-)),(0 or 1 or B)[,X]<CR>
```

The extended test option X accumulates error counts over a number of passes.

ESC key will abort test in progress

If stop on error option is selected (in answer to a prompt) the user may choose -

```
C continue
L loop
R reset stop on error
```

if an error stop occurs.

Error Reporting

Error printouts take the following form :-

```
<drive no.> <error type> <track no> /<physical sector no> <*>
```

```
Presence of '*' indictes a "hard" disc error
e.g.  1 E3 1F /0325 *
means :-        drive no 1
                error type 3 (e3)
                track no 1f
                p.s.n 0325
                error was not recoverable on retry (*)
```

If after three retries the error still persists, it will be logged as a hard error (indicated by *).

Error types are as follows (per QDOS ROM codes) :-

```
E1 data CRC error
E2 disk is write protected
E3 disk is not ready for some reason
E4 deleted data address mark read
E5 abnormal command termination
E6 invalid sector address
E7 seek error (track not found)
E8 data mark read error
E9 address mark read error
```

Additional error types are :-

E@ data read back is not the same as data written

Additional error types from the drive uniqueness test are :-

EA body of data buffer is not zero after test data
EB unique data for this drive/sector is incorrect.

Plotted Error Graphs

Errors may be summarised by use of the 'PG' command
This summary plots the track no as the vertical ordinate
and the number of errors as the horozintal ordinate.

A horizontal line may contain up to 11 error types (codes)
each character represents (n*horizontal scale) errors

The error graph is divided into two blocks. The left hand block relates to drive 0 errors, the right hand block to drive 1.

The graph is printed starting at the first track with errors logged and finishes with the last track with errors logged.

To stop the display rolling off the screen, control W can be used to stop printing. Subsequent carriage returns will print a little at a time, an escape will terminate the 'PG', and any other character will resume continuous printing.

In the case of double sided systems, each disc 'cylinder' is considered two tracks, so even track numbers correspond to side 0 of the disc and odd track numbers correspond to side 1.

Utility Commands

Commands for utility programmes are as follows

HD,d,hhhh	Head load timing test on drive d at speed hhhh (100 m.s = D8F0)
IX,d	Index sensor alignment test on drive d. t1=tk 1. t2=tk 76
AT,d,s	Read data amplitude test on drive d. s is optional side select (0 or 1). t1=tk 0. t2=tk 76
RA,d,s	Radial alignment test on drive d. s is optional side select (0 or 1) t1=0-38. t2=77-38. t3=39-38. t4=37-38.
AZ,d,s	Head azimuth test on drive d. s is optional side select. t1=0-76. t2=75-76
TO,d	Track zero sensor alignment test on drive d. t1=1-2 lp. t2=0-1 lp. t3=0-2 lp
SK,d,s	Head skew test on drive d. s is optional side select (0 or 1). t1=1-76 lp
RS,d,hhhh	Read sector hhhh from drive d to buffer
WS,d,hhhh	Write buffer to sector hhhh on drive d
DB	Display buffer in hex and ascii
FB,hhhh	Fill buffer with repeating pattern hhhh

The running test may be aborted by escape key

The next test of the sequence is entered by depressing space key
Tests followed by letters "lp" move head between tracks shown.

The drive manufacturer's manual should be consulted for information on the tests which should be applied

Some tests require the appropriate alignment diskette and ask that it be inserted

Other tests require a scratch diskette and ask that it be inserted.

Typing OS<CR> will return the user to the operating system (reboot).

DISC SYSTEM SET-UP AND DIAGNOSIS

(1) QFC-2 Floppy disc controller alignment
(2) YD-174 Disc drive set-up and alignment
(3) Disc system diagnosis

1) QFC-2 Alignment

Adustment of two separate pulse lengths is required in the data separator section of the floppy disc controller. The test signals are available at points TP1 and TP2 and adjusted by 1Ø-turn pots VR1 and VR2 respectively, on the QFC-2 board.

With a CRO set to .5uS/div and positive triggered, both signals should be high for 2.7uS when no data is being read from the disc (TP1 gets reset by data pulses).

2) YD-174 Disc Drive Pre-alignment Set-up

(1) Check that 115V motor is fitted

(2) Check that 5ØHz pulley is fitted

(3) Link 'Y' on YE Data p.c.b.

(4) Link 'C' on " " " .

(5) Move link to DS2 on p.c.b.

(6) Remove link block package and open circuit links 'X' and 'Z' (break legs off link block package)

(7) Reinstall link block

%

Disc Drive Alignment

New disc drives require the radial alignment to be checked.

(1) Place the drive on its side, with the main drive motor towards the bottom.

(2) Connect a CRO as follows to the block of test pins marked "TP" near the centre of the YE Data p.c.b.

Pin	CRO
A	Channel A
B	Channel B

3 Ext trig

(3) Set the CRO as follows:
Inputs on AC
trig on external negative
time base to 2Ø mS/div
add channels A and B
invert one channel
vertical sensitivity to 1ØØmV/div

(4) Load a disc containing the test program DSKTST and run it by typing DSKTST<CR>.

(5) Type
RA,D,S<CR> where D = drive number (Ø or 1)
S = side number (Ø or 1)

(6) Insert Alignment Disc and hit a key. This steps the head to track 38.

(7) A "double eye" pattern should appear on the CRO. The amplitudes of the two lobes must be within 7Ø% of each other.

(8) If side Ø is acceptable, repeat test for side 1

(9) If either side requires adjustment, loosen the two Philips head screws which clamp the head carriage assembly to the steel stepper motor belt. The screws are accessed through two holes in the side of the drive chassis.

(1Ø) Gently tap the carriage assembly or move the belt by hand until the lobes are within 7Ø% amplitude with the screws retightened (tightening the screws tends to change the lobe pattern), for both sides of the disc.

(11) Hit ESC to terminate the radial alignment test.

%

Track Zero Sensor Test

After the head is radially aligned, the track ØØ sensor should be checked.

(1) Still running DSKTST, type
TØ,D where D = drive (Ø or 1)

(2) Insert a scratch disc and hit any key.

(3) TØ causes the head to oscillate between track ØØ and track Ø1, Monitor the sensor signal at pin B12 of the J2 connector block on the drive p.c.b. It should oscillate with movement of the head.

(4) Terminate test by hitting ESC

%

3) Disc System Diagnosis

The general procedure to follow in disc system fault tracing is:

(1) Use the system test program CHECK to determine if the fault is in the drive itself (or the diskette) or the disc controller/DMA data transfer system.
(2) If the disc drive is faulty, use DSKTST to further analyse the fault.

Test Program CHECK

Allows checking of

- Cyclic Redundancy Check (CRC) errors
- Data transfer between memory and disc
- RAM bit corruption errors

Command Syntax

CHECK <UNIT>,<HEXNUM>;<OPTIONS>

<UNIT>::=<COLON><NUMBER>

<HEX NUMBER>::=<HEX DIGIT>|<HEX DIGIT>

<HEX DIGIT>::=<NUMBER>|A|B|C|D|E|F

<NUMBER>::=1|2|3|4|5|6|7|8|9|Ø

(1) Disc Integrity Check

Options: none required

This is the default CHECK routine. Entire disc in specified drive is read to check for CRC errors.

(2) Read Data D.M.A. Verify

Option: V

Reads entire disc in specified drive twice, into separate blocks of memory and verifies data against itself.

(3) Write Data D.M.A. Verify

Options: W,D (May be used together)

%

The W option creates a file, writes distinctive data to each sector of the file and reads each sector of the file back, twice, into different areas of memory for verification. All unfree disc space will be allocated to the file.

The D option is a destructive (to the disc contents) test which writes a unique "ADD -29" pattern to each sector in an interleaved fashion, reads it back, and verifies the data.

Interleaving of blocks ensures track boundaries are continually being crossed. A delay can be introduced using the "T" option (see below) to isolate head-load timing problems.

(4) Other Options

Option	Use with	
R	W	use random number pattern instead of "29" pattern
P=XX	W	use pattern XX where XX = <hex number> write the pattern to disc, read back and verify
E=XX	all	print error if total recoverable disc errors exceed XX where XX = <hex number>. Default value is 0.
T=XX	all	delay XX*10 ms. after a read/write where XX = <hex number>
C	all	test continously alternating between 'add-29' and a random number pattern
L	all	all error messages printed on printer

(5) Error messages

(a) Disc Read/Write Errors
These are of the form

**PROM I/O ERROR -- STATUS = <status byte> AT h DRIVE i - PSN j

where h is not significant
i = drive number
j = physical sector number at which the error occurred
and the status byte can be interpreted as follows:

31 data C.R.C. error
32 disc is write protected
33 disc is not ready for some reason

34 deleted data address mark read
35 abnormal command termination

%

36 invalid sector address
37 seek error (track not found)
38 data mark read error
39 address mark read error

(b) Verify Errors

When a verify error is encountered the offending disc sector is re-read into the QDOS sector buffer and matched against system RAM to determine where the error came from. The program then reports the corresponding address in RAM, the data expected, the erroneous data, the physical sector number of the disc where the error occured, and the byte offset within the sector.

(6) Termination

Test is terminated by -
ESC key (sets system error status word)
More then 2Ø errors logged
User supplied iteration counter expired (default 1)

System error status word will be set if any error condition has been reported.

%

Test Program DSKTST

DSKTST comprises five main test routines and a number of utility commands. The main routines are as follows -

#1 Write/read test	(destructive)
#2 Read C.R.C. test	(non-destructive)
#3 Worst case seek test	(non-destructive)
#4 Worst case data pattern R/W	(destructive)
#5 Sector/drive uniqueness	(destructive)

Tests can be run separately or in destructive/non-destruct groups by typing as follows -

DN,(Ø or 1 or B) [,X]<CR> (Do all non-destruct tests)
DD,(Ø or 1 or B) [,X]<CR> (Do all destructive tests)
ST#(up to 1Ø test no's separated by (-)),(Ø or 1 or B)[,X]<CR>

The extended test option X accumulates error counts over a number of passes.
ESC key will abort test in progress
If stop on error option is selected (in answer to a prompt) the user may choose -
C continue
L loop

R reset stop on error
if an error stop occurs.

Error Reporting

Error printouts take the following form :-

<drive no.> <error type> <track no> /<physical sector no> <*>

Presence of '*' indictes a "hard" disc error
e.g. 1 E3 1F /0325 *
means :- drive no 1
error type 3 (E3)
track no 1F
p.s.n 0325
error was not recoverable on retry (*)

If after three retries the error persists, it will be logged as a hard error (indicated by *).

Error types are as follows (per QDOS ROM codes) :-

E1 data CRC error
E2 disc is write protected
E3 disc is not ready for some reason
E4 deleted data address mark read
E5 abnormal command termination
E6 invalid sector address
E7 seek error (track not found)
E8 data mark read error
E9 address mark read error

%

Additional error types are :-
E@ data read back is not the same as data written

Additional error types from the drive uniqueness test are :-

EA body of data buffer is not zero after test data
EB unique data for this drive/sector is incorrect.

Plotted Error Graphs

Errors may be summarised by use of the 'PG' command. This summary plots the track no. as the vertical ordinate and the number of errors as the horizontal ordinate.

A horizontal line may contain up to 11 error types (codes) with each character representing (n*horizontal scale) errors.

The error graph is divided into two blocks. The left hand block relates to drive Ø errors, the right hand block to drive 1.

The graph is printed starting at the first track with errors logged and finishes with the last track with errors

logged.

To stop the display rolling off the screen, <control W> can be used to stop printing. Subsequent carriage returns will print a little at a time, an escape will terminate the 'PG', and any other character will resume continuous printing.

In the case of double sided systems, each disc 'cylinder' is considered as two tracks, so even track numbers correspond to side 0 of the disc and odd track numbers correspond to side 1.

%

Utility Commands

Commands for utility programmes are as follows

HD,d,hhhh	Head load timing test on drive d at speed hhhh (100 mS = D8F0)
IX,d	Index sensor alignment test on drive d. t1=tk 1. t2=tk 76.
AT,d,s	Read data amplitude test on drive d. s is optional side select (0 or 1). t1=tk 0. t2=tk 76.
RA,d,s	Radial alignment test on drive d. s is optional side select (0 or 1) t1=0-38. t2=77-38. t3=39-38. t4=37-38.
AZ,d,s	Head azimuth test on drive d. s is optional side select. t1=0-76. t2=75-76.
T0,d	Track zero sensor alignment test on drive d. t1=1-2 lp. t2=0-1 lp. t3=0-2 lp.
SK,d,s	Head skew test on drive d. s is optional side select (0 or 1). t1=1-76 lp.
RS,d,hhhh	Read sector hhhh from drive d to buffer
WS,d,hhhh	Write buffer to sector hhhh on drive d
DB	Display buffer in hex and ascii
FB,hhhh	Fill buffer with repeating pattern hhhh

The running test may be aborted by escape key

The next test of the sequence is entered by depressing space key Tests followed by letters "lp" move head between tracks shown.

The drive manufacturer's manual should be consulted for information on the tests which should be applied

Some tests require the appropriate alignment diskette and ask that it be inserted

Other tests require a scratch discette and ask that it be inserted.

Typing OS<CR> will return the user to the operating system (reboot).

FAIRLIGHT INSTRUMENTS PTY. LTD.
15 BOUNDARY STREET RUSHCUTTERS BAY.
SYDNEY, AUSTRALIA 2011 Ph. (02) 335222
TELEX: AA27998

FIELD CHANGE NOTICE

FCN No 50

DATE 5th Oct. 1982 BY AJC

MODEL No. EPSON PRINTER REVISION SERIAL INTERFACE CARD TYPE 2

SERIAL No. EFFECTED

REASON FOR MODIFICATION

ALLOW EPSON PRINTER TO BE USED WITH CMI
(Q-032 DEBUG CARD)

MODIFICATION/CHANGE REQUIRED

Remove Serial Interface card from printer

Solder Side of Card

1. Isolate pins 11, 12, 13 of IC/3A (4075) from ground and each other
2. Cut track from pin 6 of IC/2B (75189) to jumper J2.
3. Re-connect J2 to pin 10 of IC/3A (4075)
4. Re-connect pin 6 of IC/2B (75189) to pins 12 & 13 of IC/3A (4075)
5. Connect pin 11 of 4075 to pin 3 of 75189

Replace Card in printer.

DRAWING ATTACHED YES ☑ NO ☐

OVERLAYS ATTACHED YES ☑ NO ☐

...ocations

...u shows the component layout of the Serial Interface Board. (Cat. No. .46).

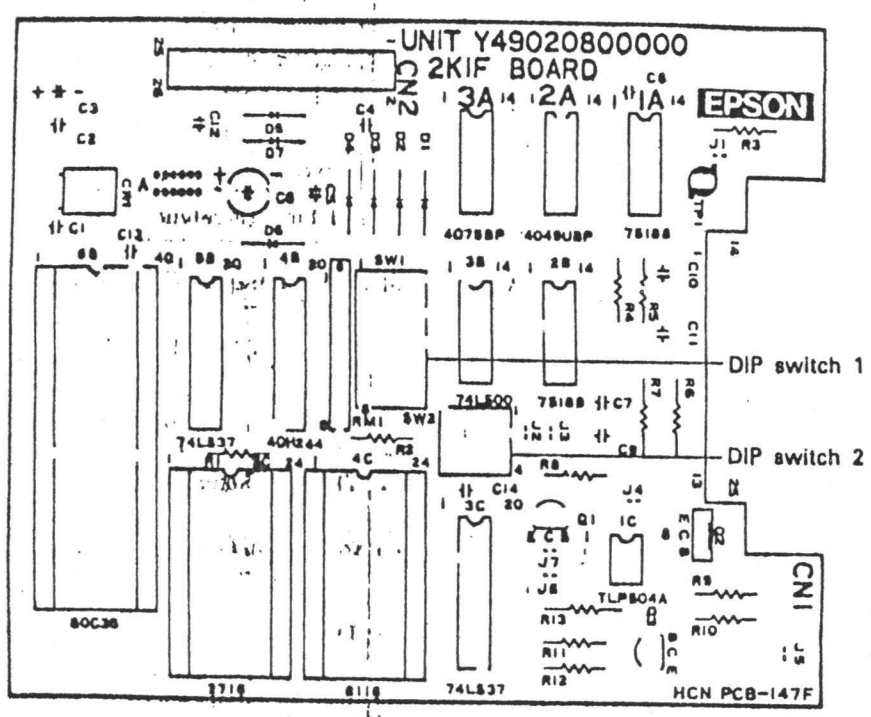


Fig. 6 Component Layout

(5) Schematic Diagram

Fig. 7 shows the schematic diagram of the Serial Interface Board (Cat. No. 8145).

— CIRCUIT MOD FOR CMI —

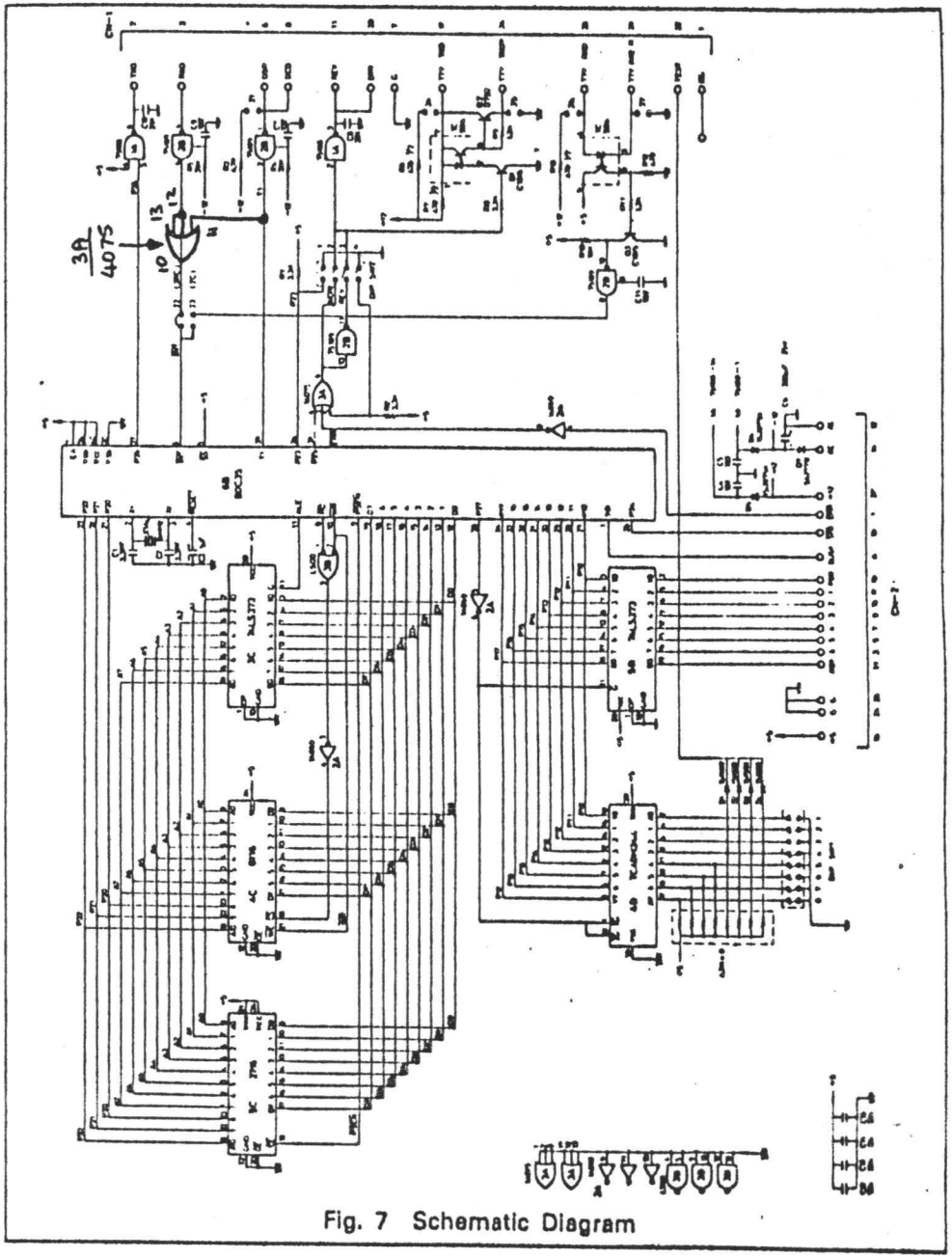
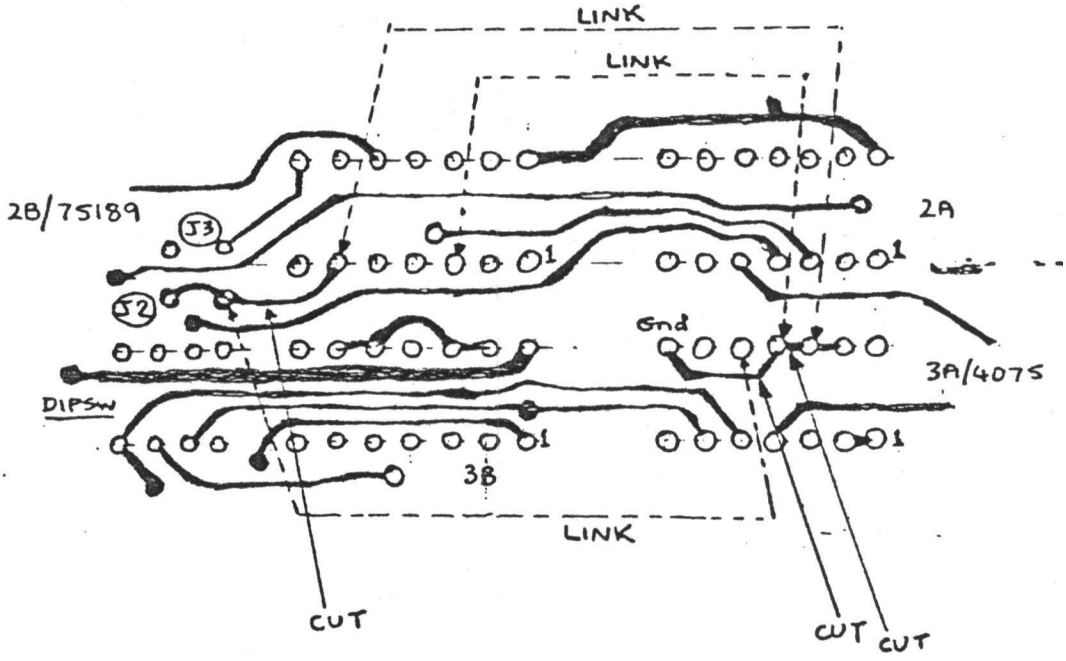


Fig. 7 Schematic Diagram

WIRING SIDE



EPSON RS232C/CURRENT LOOP INTERFACE
TYPE 2

P.C MODS FOR USE WITH CMI

CMI - EPSON PRINTER

CABLE CONNECTIONS

CMI 5-PIN CANNON	SIGNAL NAME	EPSON PIN
1	GROUND	7
2	N.C.	
3	DTR	20
4	DEVICE ON	6
5	DATA	3.

SWITCH SETTINGS

SW1

1	ON	
2	OFF	*
3	OFF	*
4	OFF	
5	ON	
6	ON	
7	ON	*
8	ON	

SW2

1	OFF	*
2	ON	
3	OFF	
4	ON	

*: Change from Factory Setting

M E M O

To: Will Alexander
From: Dave Bross
Re: Channel Card Replacement

Date: 13 July 1982

Kim Ryrie advises that some of our systems have already been upgraded with new or modified channel cards.

Could you please advise Australia the following:

a). Serial numbers of all systems needing channel card upgrades.

b). Revision number I.D.'s for all channel cards in the above identified systems.

As discussed earlier, Australia agrees to suitably modify (or replace) the affected cards.

cc: Ed Matthews

DB:ij